1M × 4 BANKS × 32 BITS GDDR SDRAM

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1. GENERAL DESCRIPTION

W9412G2IB is a CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM); organized as 1,048,576 words × 4 banks × 32 bits. W9412G2IB delivers a data bandwidth of up to 500M words per second (-4). To fully comply with the personal computer industrial standard, W9412G2IB is sorted into following speed grades: -4, -5, -5I, -6 and -6I. The -4 is compliant to the DDR500/CL3 or CL4 specification. The -5/-5I is compliant to the DDR400/CL3 specification (-5I grade which is guaranteed to support -40°C ~ 85°C). The -6/-6I is compliant to the DDR333/CL2.5 specification (-6I grade which is guaranteed to support -40°C ~ 85°C).

All Input reference to the positive edge of CLK (except for DQ, DM and CKE). The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition. Write and Read data are synchronized with the both edges of DQS (Data Strobe).

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9412G2IB is ideal for any high performance applications.

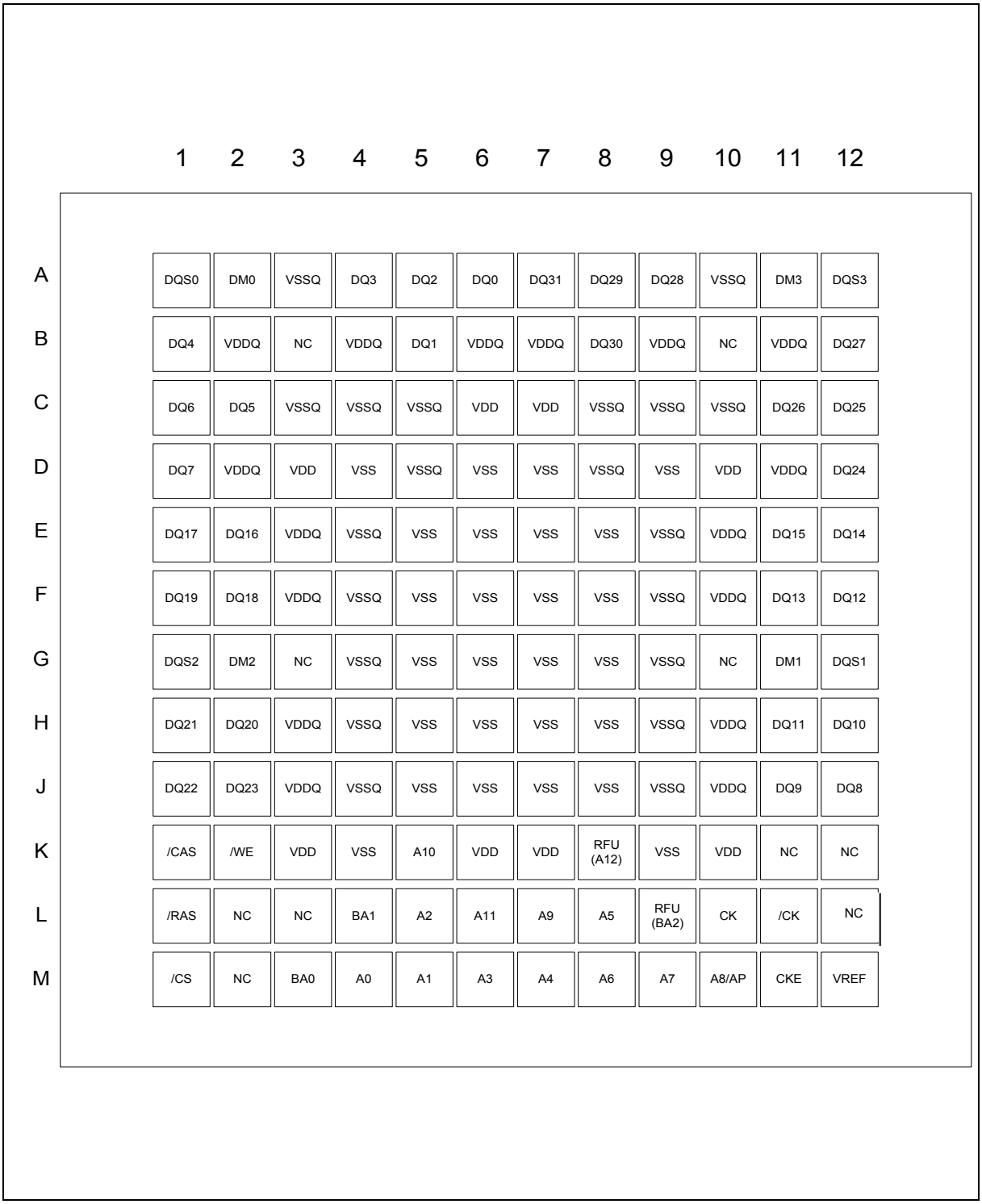
2. FEATURES

- 2.5V ±0.2V Power Supply for DDR 333/400
- 2.5V ±0.1V Power Supply for DDR500
- Up to 250 MHz Clock Frequency
- Double Data Rate architecture; two data transfers per clock cycle
- Differential clock inputs (CLK and $\overline{CLK}$)
- DQS is edge-aligned with data for Read; center-aligned with data for Write
- CAS Latency: 2, 2.5, 3 and 4
- Burst Length: 2, 4 and 8
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- 15.6μS Refresh interval (4K/64 mS Refresh)
- Maximum burst refresh cycle: 8
- Interface: SSTL_2
- Packaged in 144L LFBGA, using Lead free materials with RoHS compliant

3. KEY PARAMETERS

SYMBOL	DESCRIPTION		MIN./MAX.	-4	-5/-5I	-6/-6I
t_{CK}	Clock Cycle Time	CL = 2	Min.	-	7.5 nS	7.5 nS
			Max.	-	12 nS	12 nS
		CL = 2.5	Min.	-	6 nS	6 nS
			Max.	-	12 nS	12 nS
		CL = 3	Min.	4 nS	5 nS	6 nS
			Max.	12 nS	12 nS	12 nS
		CL = 4	Min.	4 nS	-	-
			Max.	12 nS	-	-
t_{RAS}	Active to Precharge Command Period		Min.	40 nS	40 nS	42 nS
t_{RC}	Active to Ref/Active Command Period		Min.	48 nS	50 nS	54 nS
I_{DD0}	Operating Current: One Bank Active-Precharge		Max.	160 mA	150 mA	140 mA
I_{DD1}	Operating Current: One Bank Active-Read-Precharge		Max.	180 mA	170 mA	160 mA
I_{DD4R}	Burst Operation Read Current		Max.	240 mA	220 mA	200 mA
I_{DD4W}	Burst Operation Write Current		Max.	270 mA	250 mA	230 mA
I_{DD5}	Auto Refresh Current		Max.	210 mA	200 mA	190 mA
I_{DD6}	Self-Refresh Current		Max.	3 mA	3 mA	3 mA

4. BALL CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	12
A	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
B	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
C	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
D	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
E	DQ17	DQ16	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ15	DQ14
F	DQ19	DQ18	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ13	DQ12
G	DQS2	DM2	NC	VSSQ	VSS	VSS	VSS	VSS	VSSQ	NC	DM1	DQS1
H	DQ21	DQ20	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ11	DQ10
J	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
K	/CAS	/WE	VDD	VSS	A10	VDD	VDD	RFU (A12)	VSS	VDD	NC	NC
L	/RAS	NC	NC	BA1	A2	A11	A9	A5	RFU (BA2)	CK	/CK	NC
M	/CS	NC	BA0	A0	A1	A3	A4	A6	A7	A8/AP	CKE	VREF

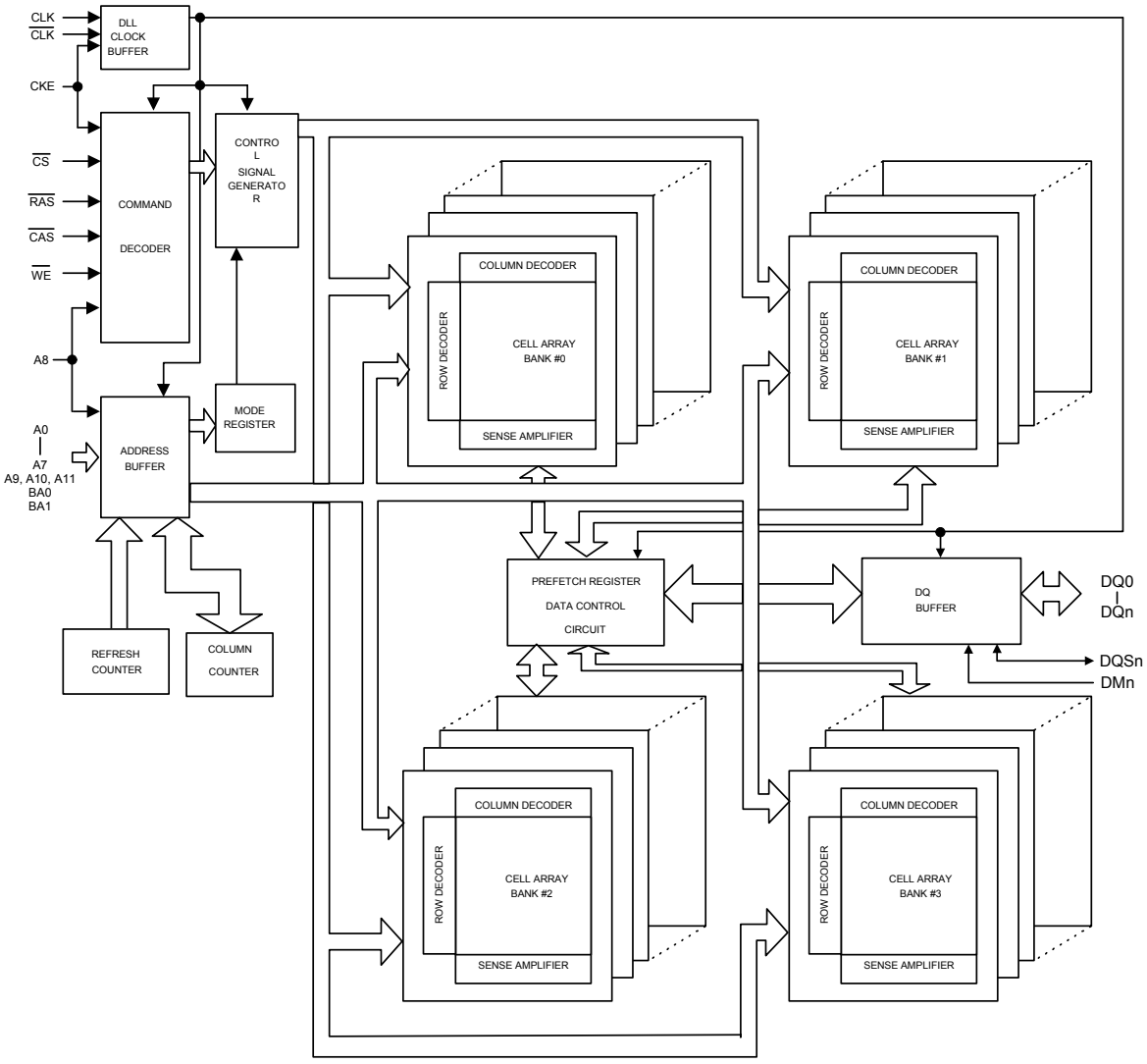
5. BALL DESCRIPTION

BALL LOCATION	PIN NAME	FUNCTION	DESCRIPTION
M4-M10, L5-L8, K5	A0–A11	Address	Multiplexed pins for row and column address. Row address: A0–A11. Column address: A0–A7. (A8 is used for Auto-precharge)
M3, L4	BA0, BA1	Bank Address	Select bank to activate during row address latch time, or bank to read/write during column address latch time.
A4-A9,B1,B5,B8, B12,C1,C2,C11,C12,D1,D12,E1,E2,E11,E12,F1,F2,F11,F12,H1,H2,H11,H12,J1,J2,J11,J12	DQ0–DQ31	Data Input/ Output	The DQ0–DQ31 input and output data are synchronized with both edges of DQS.
A1,A12,G1,G12	DQS0–DQS3	Data Strobe	DQS is Bi-directional signal. DQS is input signal during write operation and output signal during read operation. It is Edge-aligned with read data, Center-aligned with write data.
M1	$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
K1,K2,L1	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Command Inputs	Command inputs (along with $\overline{CS}$) define the command being entered.
A2,A11,G2,G11	DM0–DM3	Write mask	DM is an input mask signal for writes data. When DM is asserted “high” in burst write, the input data is masked. DM is synchronized with both edges of DQS.
L10,L11	CLK, $\overline{CLK}$	Differential clock inputs	All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{CLK}$.
M11	CKE	Clock Enable	CKE controls the clock activation and deactivation. CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CLK, $\overline{CLK}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH.
M12	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
C6,C7,D3,D10,K3,K6, K7,K10	V_{DD}	Power (+2.5V)	Power for logic circuit inside DDR SDRAM.

BALL DESCRIPTION, continued

BALL LOCATION	PIN NAME	FUNCTION	DESCRIPTION
D4,D6,D7,D9, E5~E8,F5~F8,G5~ G8,H5~H8,J5~J8,K 4,K9	V_{SS}	Ground	Ground for logic circuit inside DDR SDRAM.
B2,B4,B6,B7, B9,B11,D2,D11,E3, E10,F3,F10,H3,H10 ,J3,J10	V_{DDQ}	Power (+ 2.5V) for I/O buffer	Separated power from V_{DD}, used for output buffer, to improve noise immunity.
A3,A10,C3~C5, C8~C10,D5,D8,E4, E9,F4,F9,G4,G9,H4 ,H9,J4,J9	V_{SSQ}	Ground for I/O buffer	Separated ground from V_{SS}, used for output buffer, to improve noise immunity.
B3,B10,G3,G10,K1 1,K12,L2,L3,L12,M 2	NC	No Connection	No connection
K8,L9	RFU	No Connection	Reserved for Future Use.

6. BLOCK DIAGRAM



NOTE: The cell array configuration is 4096 * 256 * 32

7. FUNCTIONAL DESCRIPTION

7.1 Power Up Sequence

(1) Apply power and attempt to CKE at a low state (≤0.2V), all other inputs may be undefined
   1) Apply V_{DD} before or at the same time as V_{DDQ}.
   2) Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}.

(2) Start Clock and maintain stable condition for 200 µS (min.).

(3) After stable power and clock, apply NOP and take CKE high.

(4) Issue precharge command for all banks of the device.

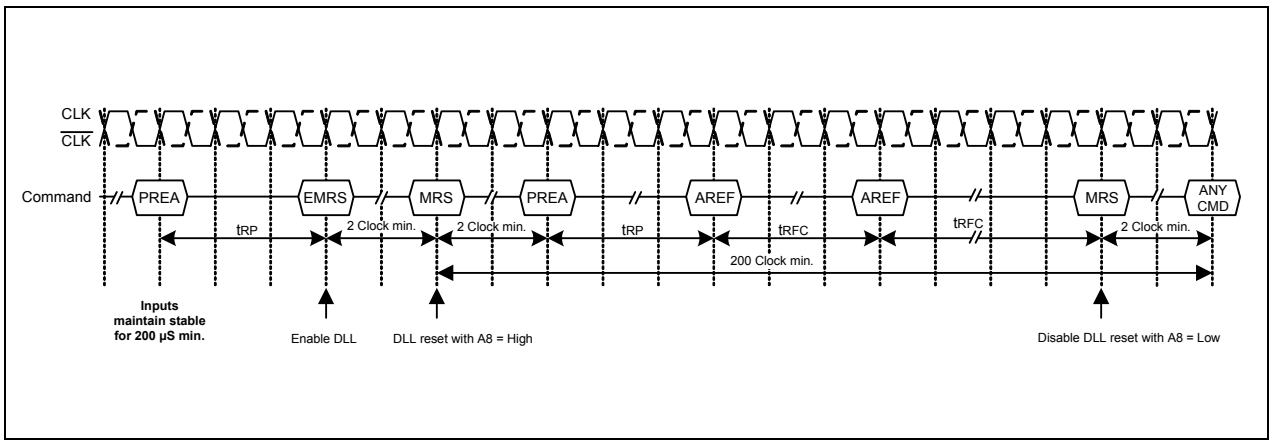
(5) Issue EMRS (Extended Mode Register Set) to enable DLL and establish Output Driver Type.

(6) Issue MRS (Mode Register Set) to reset DLL and set device to idle with bit A8.
(An additional 200 cycles(min) of clock are required for DLL Lock before any executable command applied.)

(7) Issue precharge command for all banks of the device.

(8) Issue two or more Auto Refresh commands.

(9) Issue MRS-Initialize device operation with the reset DLL bit deactivated A8 to low.



Initialization sequence after power-up

7.2 Command Function

7.2.1 Bank Activate Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", BA0, BA1 = Bank, A0 to A11 = Row Address)

The Bank Activate command activates the bank designated by the BA (Bank address) signal. Row addresses are latched on A0 to A11 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as $t_{RAS\ (max)}$. After this command is issued, Read or Write operation can be executed.

7.2.2 Bank Precharge Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BA0, BA1 = Bank, A8 = "L", A0 to A7, A9 to A11 = Don't Care)

The Bank Precharge command percharges the bank designated by BA. The precharged bank is switched from the active state to the idle state.

7.2.3 Precharge All Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BA0, BA1 = Don't Care, A8 = "H", A0 to A7, A9 to A11 = Don't Care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

7.2.4 Write Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0, BA1 = Bank, A8 = "L", A0 to A7 = Column Address)

The write command performs a Write operation to the bank designated by BA. The write data are latched at both edges of DQS. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be in the Mode Register at power-up prior to the Write operation.

7.2.5 Write with Auto-precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0, BA1 = Bank, A8 = "H", A0 to A7 = Column Address)

The Write with Auto-precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

7.2.6 Read Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BA0, BA1 = Bank, A8 = "L", A0 to A7 = Column Address)

The Read command performs a Read operation to the bank designated by BA. The read data are synchronized with both edges of DQS. The length of read data (Burst Length), Addressing Mode and CAS Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

7.2.7 Read with Auto-precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BA0, BA1 = Bank, A8 = "H", A0 to A7 = Column Address)

The Read with Auto-precharge command automatically performs the Precharge operation after the Read operation.

1) READA ≥ $t_{RAS\ (min)}$ – (BL/2) x t_{CK}

Internal precharge operation begins after BL/2 cycle from Read with Auto-precharge command.

2) $t_{RCD(min)}$ ≤ READA < $t_{RAS(min)}$ – (BL/2) x t_{CK}

Data can be read with shortest latency, but the internal Precharge operation does not begin until after $t_{RAS\ (min)}$ has completed.

This command must not be interrupted by any other command.

7.2.8 Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "L", A0 to A11 = Register Data)

The Mode Register Set command programs the values of CAS Latency, Addressing Mode, Burst Length and DLL reset in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

7.2.9 Extended Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "L", A0 to A11 = Register data)

The Extended Mode Register Set command can be implemented as needed for function extensions to the standard (SDR-SDRAM). Currently the only available mode in EMRS is DLL enable/disable, decoded by A0. The default value of the extended mode register is not defined; therefore this command must be issued during the power-up sequence for enabling DLL. Refer to the table for specific codes.

7.2.10 No-Operation Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H")

The No-Operation command simply performs no operation (same command as Device Deselect).

7.2.11 Burst Read Stop Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "L")

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

7.2.12 Device Deselect Command

($\overline{CS}$ = "H")

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

7.2.13 Auto Refresh Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "H", BA0, BA1, A0 to A11 = Don't Care)

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS–BEFORE–RAS (CBR) refresh in previous DRAM types. This command is non-persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of t_{REFI} (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * t_{REFI}.

7.2.14 Self Refresh Entry Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "L", BA0, BA1, A0 to A11 = Don't Care)

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH. Since CKE is an SSTL_2 input, V_{REF} must be maintained during SELF REFRESH.

7.2.15 Self Refresh Exit Command

(CKE = "H", $\overline{CS}$ = "H" or CKE = "H", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H")

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFREH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

7.2.16 Data Write Enable /Disable Command

(DM = "L/H" or DM0–DM3 = "L/H")

During a Write cycle, the DM0–DM3, DMs signal functions as Data Mask and can control every word of the input data. The DM0 signal controls DQ0 to DQ7, DM1 signal controls DQ8 to DQ15, DM2 signal controls DQ16 to DQ23 and DM3 signal controls DQ24 to DQ31.

7.3 Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized with both edges of DQS (Burst Read operation). The initial read data becomes available after CAS Latency from the issuing of the Read command. The CAS Latency must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst Read and operation, the Burst operation is terminated.

When the Read with Auto-precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.

7.4 Write Operation

Issuing the Write command after t_{RCD} from the bank activate command. The input data is latched sequentially, synchronizing with both edges (rising & falling) of DQS after the Write command (Burst write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto-precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state, The Write with Auto-precharge command cannot be interrupted by any other command for the entire burst data duration.

Refer to the diagrams for Write operation.

7.5 Precharge

There are two Commands, which perform the precharge operation (Bank Precharge and Precharge All). When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as $t_{RAS\ (max)}$. Therefore, each bank must be precharged within $t_{RAS(max)}$ from the bank activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharge bank is then switched to the idle state.

7.6 Burst Termination

When the Precharge command is used for a bank in a Burst cycle, the Burst operation is terminated. When Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of (CAS Latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset at the same clock cycle at which the precharge command is issued. In this case, the DM signal must be asserted “high” during t_{WR} to prevent writing the invalided data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst read Stop command is not supported during a write burst operation. Refer to the diagrams for Burst termination.

7.7 Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 4096 times (rows) within 64mS. The period between the Auto Refresh command and the next command is specified by t_{RFC}.

Self Refresh mode enter issuing the Self Refresh command (CKE asserted “low”), while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE held “low”. In the case of distributed Auto Refresh commands, distributed auto refresh commands must be issued every 15.6 µS and the last distributed Auto Refresh commands must be performed within 15.6 µS before entering the self refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 15.6 µS. In Self Refresh mode, all input/output buffers are disabled,

resulting in lower power dissipation (except CKE buffer). Refer to the diagrams for Refresh operation.

7.8 Power Down Mode

Two types of Power Down Mode can be performed on the device: Active Power Down Mode and Precharge Power Down Mode.

When the device enters the Power Down Mode, all input/output buffers are disabled resulting in low power dissipation (except CKE buffer).

Power Down Mode enter asserting CKE “low” while the device is not running a burst cycle. Taking CKE “high” can exit this mode. When CKE goes high, a No operation command must be input at next CLK rising edge. Refer to the diagrams for Power Down Mode.

7.9 Input Clock Frequency Change during Precharge Power Down Mode

DDR SDRAM input clock frequency can be changed under following condition:

DDR SDRAM must be in precharged power down mode with CKE at logic LOW level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequency specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before precharge power down mode may be exited. The DLL must be RESET via EMRS after precharge power down exit. An additional MRS command may need to be issued to appropriately set CL etc. After the DLL relock time, the DRAM is ready to operate with new clock frequency.

7.10 Mode Register Operation

The mode register is programmed by the Mode Register Set command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0 to A11 and BA0, BA1 address inputs.

The Mode Register designates the operation mode for the read or write cycle. The register is divided into five filed: (1) Burst Length field to set the length of burst data (2) Addressing Mode selected bit to designate the column access sequence in a Burst cycle (3) CAS Latency field to set the assess time in clock cycle (4) DLL reset field to reset the DLL (5) Regular/Extended Mode Register filed to select a type of MRS (Regular/Extended MRS). EMRS cycle can be implemented the extended function (DLL enable/Disable mode).

The initial value of the Mode Register (including EMRS) after power up is undefined; therefore the Mode Register Set command must be issued before power operation.

7.10.1 Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2, 4, 8 words.

A2	A1	A0	BURST LENGTH
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	x	x	Reserved

7.10.2 Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential Mode, When the A3 bit is “0”, Sequential mode is selected. When the A3 bit is “1”, Interleave mode is selected. Both addressing Mode support burst length 2, 4 and 8 words.

A3	ADDRESSING MODE
0	Sequential
1	Interleave

- **Addressing Sequence of Sequential Mode**

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.

Addressing Sequence of Sequential Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is A0)
Data 1	n + 1	not carried from A0 to A1
Data 2	n + 2	4 words (address bit A0, A1)
Data 3	n + 3	Not carried from A1 to A2
Data 4	n + 4	
Data 5	n + 5	8 words (address bits A2, A1 and A0)
Data 6	n + 6	Not carried from A2 to A3
Data 7	n + 7	

- **Addressing Sequence of Interleave Mode**

  A Column access is started from the inputted column address and is performed by interleaving the address bits in the sequence shown as the following.

Address Sequence for Interleave Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	8 words
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

7.10.3 CAS Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of CAS Latency depend on the frequency of CLK.

A6	A5	A4	CAS LATENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

7.10.4 DLL Reset bit (A8)

This bit is used to reset DLL. When the A8 bit is “1”, DLL is reset.

7.10.5 Mode Register /Extended Mode register change bits (BA0, BA1)

These bits are used to select MRS/EMRS.

BA1	BA0	A11–A0
0	0	Regular MRS Cycle
0	1	Extended MRS Cycle
1	x	Reserved

7.10.6 Extended Mode Register field

1) DLL Switch field (A0)

This bit is used to select DLL enable or disable

A0	DLL
0	Enable
1	Disable

2) Output Driver Strength Control field (A6, A1)

The 100%, 60% and 30% or matched impedance driver strength are required Extended Mode Register Set (EMRS) as the following:

A6	A1	BUFFER STRENGTH
0	0	100% Strength
0	1	60% Strength
1	0	Reserved
1	1	30% Strength

7.10.7 Reserved field

- Test mode entry bit (A7)
  This bit is used to enter Test mode and must be set to “0” for normal operation.
- Reserved bits (A9, A10, A11)
  These bits are reserved for future operations. They must be set to “0” for normal operation.

8. OPERATION MODE

The following table shows the operation commands.

8.1 Simplified Truth Table

SYM.	COMMAND	DEVICE STATE	CKE_{n-1}	CKE_n	DM(4)	BA0,BA1	A8	A0-A7 A9-A11	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank Active	Idle(3)	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any(3)	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active(3)	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Auto-precharge	Active(3)	H	X	X	V	H	V	L	H	L	L
READ	Read	Active(3)	H	X	X	V	L	V	L	H	L	H
READA	Read with Auto-precharge	Active(3)	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	L, L	C	C	L	L	L	L
EMRS	Extended Mode Register Set	Idle	H	X	X	H, L	V	V	L	L	L	L
NOP	No Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst Read Stop	Active	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
PD	Power Down Mode Entry	Idle/ Active(5)	H	L	X	X	X	X	H	X	X	X
									L	H	H	X
PDEX	Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
WDE	Data Write Enable	Active	H	X	L	X	X	X	X	X	X	X
WDD	Data Write Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V = Valid X = Don't Care L = Low level H = High level
2. CKE_n signal is input level when commands are issued.
   CKE_{n-1} signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BA0, BA1 signals.
4. DM0–DM3 (W9412G2IB).
5. Power Down Mode can not entry in the burst cycle.

8.2 Function Truth Table

(Note 1)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A8	PRE/PREA	NOP	
	L	L	L	H	X	AREF/SELF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode register accessing	2
Row Active	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A8	READ/READA	Begin read: Determine AP	4
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Begin write: Determine AP	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	Precharge	5
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BA, CA, A8	READ/READA	Term burst, new read: Determine AP	6
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	Term burst, precharging	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	Term burst, start read: Determine AP	6, 7
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Term burst, start read: Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	Term burst, Precharging	8
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

8.3 Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Read with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharging	H	X	X	X	X	DSL	NOP-> Idle after t_{RP}	
	L	H	H	H	X	NOP	NOP-> Idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	Idle after t_{RP}	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	NOP-> Row active after t_{RCD}	
	L	H	H	H	X	NOP	NOP-> Row active after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

8.4 Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Write Recovering	H	X	X	X	X	DSL	NOP->Row active after t_{WR}	
	L	H	H	H	X	NOP	NOP->Row active after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write Recovering with Auto-precharge	H	X	X	X	X	DSL	NOP->Enter precharge after t_{WR}	
	L	H	H	H	X	NOP	NOP->Enter precharge after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A8	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A8	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	NOP->Idle after t_{RC}	
	L	H	H	H	X	NOP	NOP->Idle after t_{RC}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PREA	ILLEGAL	
	L	L	L	X	X	AREF/SELF/MRS/EMRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DSL	NOP->Row after t_{MRD}	
	L	H	H	H	X	NOP	NOP->Row after t_{MRD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PREA/AREF/SELF/MRS/EMRS	ILLEGAL	

Notes:

1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Illegal if t_{RCD} is not satisfied.
5. Illegal if t_{RAS} is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don't satisfy t_{WR}

Remark: H = High level, L = Low level, X = High or Low level (Don't Care), V = Valid data

8.5 Function Truth Table for CKE

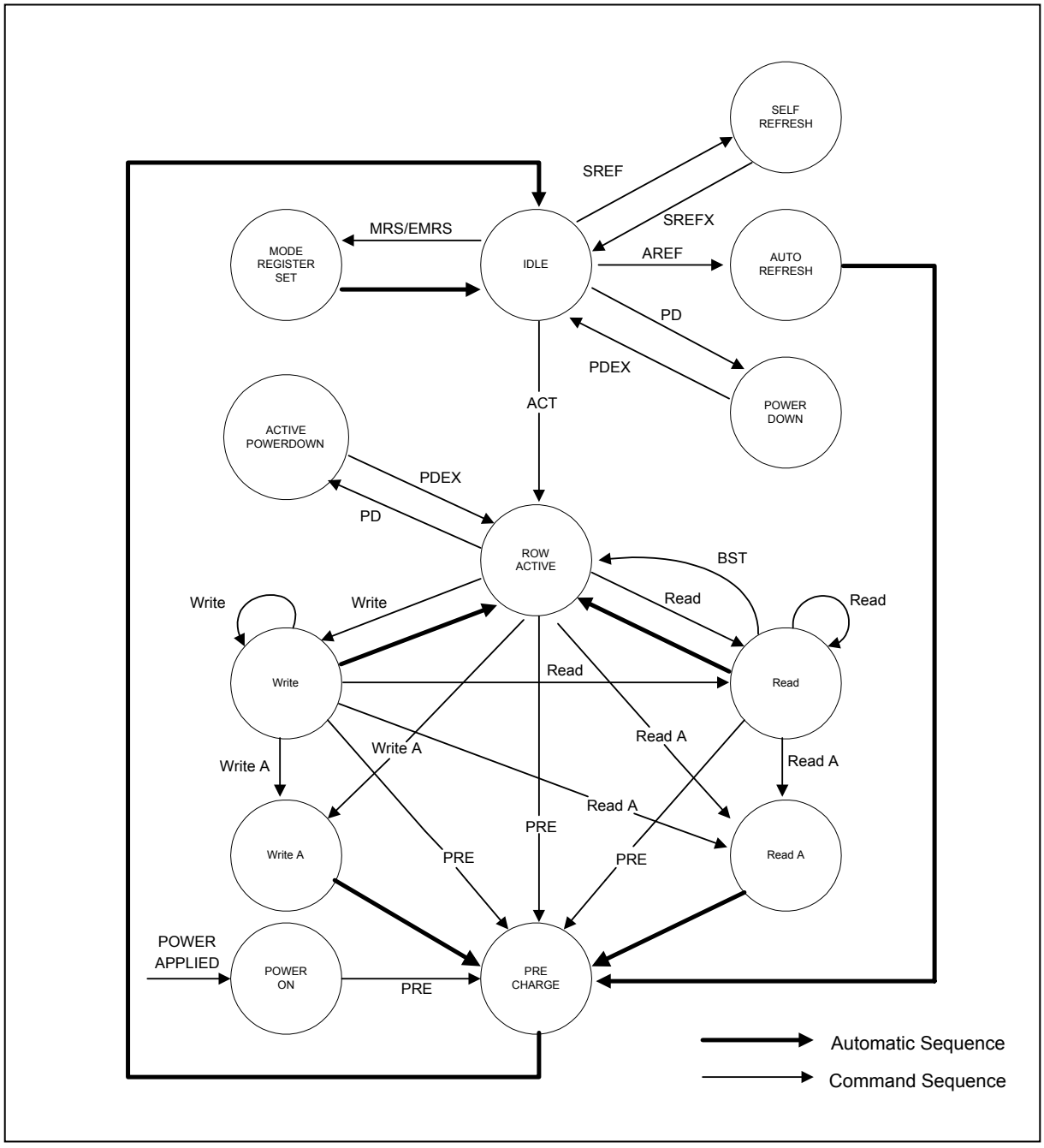
CURRENT STATE	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	ACTION	NOTES
	n-1	n							
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh->Idle after t_{XSNR}	
	L	H	L	H	H	X	X	Exit Self Refresh->Idle after t_{XSNR}	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power down->Idle after t_{IS}	
	L	L	X	X	X	X	X	Maintain power down mode	
All banks Idle	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	Self Refresh	1
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Row Active	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	3
	H	L	L	H	H	X	X	Enter Power down	3
	H	L	L	L	L	H	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Any State Other Than Listed Above	H	H	X	X	X	X	X	Refer to Function Truth Table	

Notes:

1. Self refresh can enter only from the all banks idle state.
2. Power Down occurs when all banks are idle; this mode is referred to as precharge power down.
3. Power Down occurs when there is a row active in any bank; this mode is referred to as active power down.

Remark: H = High level, L = Low level, X = High or Low level (Don't Care), V = Valid data

8.6 Simplified Stated Diagram



9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Input/Output Voltage	V_{IN}, V_{OUT}	-0.3 ~ V_{DDQ} + 0.3	V
Power Supply Voltage	V_{DD}, V_{DDQ}	-0.3 ~ 3.6	V
Operating Temperature (-4/-5/-6)	T_{OPR}	0 ~ 70	°C
Operating Temperature (-5I/-6I)	T_{OPR}	-40 ~ 85	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C
Soldering Temperature (10s)	T_{SOLDER}	260	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OUT}	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9.2 Recommended DC Operating Conditions

(T_A = 0 to 70°C for -4/-5/-6, T_A = -40 to 85°C for -5I/-6I)

SYM.	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage (for -5/-5I/-6/-6I)	2.3	2.5	2.7	V	2
V_{DD}	Power Supply Voltage (for -4)	2.4	2.5	2.6	V	2
V_{DDQ}	I/O Buffer Supply Voltage (for -5/-5I/-6/-6I)	2.3	2.5	2.7	V	2
V_{DDQ}	I/O Buffer Supply Voltage (for -4)	2.4	2.5	2.6	V	2
V_{REF}	Input reference Voltage	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage (System)	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	2, 8
$V_{IH\ (DC)}$	Input High Voltage (DC)	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	2
$V_{IL\ (DC)}$	Input Low Voltage (DC)	-0.3	-	V_{REF} - 0.15	V	2
$V_{ICK\ (DC)}$	Differential Clock DC Input Voltage	-0.3	-	V_{DDQ} + 0.3	V	15
$V_{ID\ (DC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.36	-	V_{DDQ} + 0.6	V	13, 15
$V_{IH\ (AC)}$	Input High Voltage (AC)	V_{REF} + 0.31	-	-	V	2
$V_{IL\ (AC)}$	Input Low Voltage (AC)	-	-	V_{REF} - 0.31	V	2
$V_{ID\ (AC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.7	-	V_{DDQ} + 0.6	V	13, 15
$V_{X\ (AC)}$	Differential AC input Cross Point Voltage	V_{DDQ}/2 - 0.2	-	V_{DDQ}/2 + 0.2	V	12, 15
$V_{ISO\ (AC)}$	Differential Clock AC Middle Point	V_{DDQ}/2 - 0.2	-	V_{DDQ}/2 + 0.2	V	14, 15

Notes: Undershoot Limit: V_{IL} (min) = -1.5V with a pulse width $\leq$ 5 nS

Overshoot Limit: V_{IH} (max) = V_{DDQ} +1.5V with a pulse width $\leq$ 5 nS

$V_{IH\ (DC)}$ and $V_{IL\ (DC)}$ are levels to maintain the current logic state.

$V_{IH\ (AC)}$ and $V_{IL\ (AC)}$ are levels to change to the new logic state.

9.3 Capacitance

(V_{DD} = V_{DDQ} = 2.5V ±0.2V, f = 1 MHz, T_A = 25 °C, $V_{OUT\ (DC)}$ = V_{DDQ}/2, V_{OUT} (Peak to Peak) = 0.2V)

SYMBOL	PARAMETER	MIN.	MAX.	DELTA (MAX.)	UNIT
C_{IN}	Input Capacitance (except for CLK pins)	2.0	4.0	0.5	pF
C_{CLK}	Input Capacitance (CLK pins)	3.0	5.5	0.25	pF
$C_{I/O}$	DQ, DQS, DM Capacitance	1.5	5.5	0.5	pF
C_{NC}	NC Pin Capacitance	-	1.5	-	pF

Notes: These parameters are periodically sampled and not 100% tested.

The NC pins have additional capacitance for adjustment of the adjacent pin capacitance.

9.4 Leakage and Output Buffer Characteristics

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
$I_{I\ (L)}$	Input Leakage Current (0V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0V)		-2	2	µA	
$I_{O\ (L)}$	Output Leakage Current (Output disabled, 0V ≤ V_{OUT} ≤ V_{DDQ})		-5	5	µA	
V_{OH}	Output High Voltage (under AC test load condition)	100% Strength	V_{TT} +0.76	-	V	
V_{OL}	Output Low Voltage (under AC test load condition)		-	V_{TT} -0.76	V	
$I_{OH\ (DC)}$	Output Minimum Source DC Current		-15.2	-	mA	4, 6
$I_{OL\ (DC)}$	Output Minimum Sink DC Current		15.2	-	mA	4, 6
$I_{OH\ (DC)}$	Output Minimum Source DC Current	60% Strength	-10.4	-	mA	5
$I_{OL\ (DC)}$	Output Minimum Sink DC Current		10.4	-	mA	5
$I_{OH\ (DC)}$	Output Minimum Source DC Current	30% Strength	-7.2	-	mA	5
$I_{OL\ (DC)}$	Output Minimum Sink DC Current		7.2		mA	5

9.5 DC Characteristics

SYM.	PARAMETER	MAX.			UNIT	NOTES
		-4	-5/-5I	-6/-6I		
I_{DD0}	Operating current: One Bank Active-Precharge; t_{RC} = t_{RC} min; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	160	150	140	mA	7
I_{DD1}	Operating current: One Bank Active-Read-Precharge; Burst = 2; t_{RC} = t_{RC} min; CL = 3; t_{CK} = t_{CK} min; I_{OUT} = 0 mA; Address and control inputs changing once per clock cycle.	180	170	160	mA	7, 9
I_{DD2P}	Precharge Power Down standby current: All Banks Idle; Power down mode; CKE $\leq$ V_{IL} max; t_{CK} = t_{CK} min; Vin = V_{REF} for DQ, DQS and DM	30	30	30	mA	
I_{DD2N}	Idle standby current: $\overline{CS}$ $\geq$ V_{IH} min; All Banks Idle; CKE $\geq$ V_{IH} min; t_{CK} = t_{CK} min; Address and other control inputs changing once per clock cycle; Vin $\geq$ V_{IH} min or Vin $\leq$ V_{IL} max for DQ, DQS and DM	45	45	45	mA	7
I_{DD3P}	Active Power Down standby current: One Bank Active; Power down mode; CKE $\leq$ V_{IL} max; t_{CK} = t_{CK} min	30	30	30	mA	
I_{DD3N}	Active standby current: $\overline{CS}$ $\geq$ V_{IH} min; CKE $\geq$ V_{IH} min; One Bank Active-Precharge; t_{RC} = t_{RAS} max; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	60	60	60	mA	7
I_{DD4R}	Operating current: Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL=3; t_{CK} = t_{CK} min; I_{OUT} = 0mA	240	220	200	mA	7, 9
I_{DD4W}	Operating current: Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 3; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle	270	250	230	mA	7
I_{DD5}	Auto Refresh current: t_{RC} = t_{RFC} min	210	200	190	mA	7
I_{DD6}	Self Refresh current: CKE $\leq$ 0.2V	3	3	3	mA	
I_{DD7}	Random Read current: 4 Banks Active Read with activate every 20nS, Auto-Precharge Read every 20 nS; Burst = 4; t_{RCD} = 3; I_{OUT} = 0mA; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	340	320	300	mA	

9.6 AC Characteristics and Operating Condition

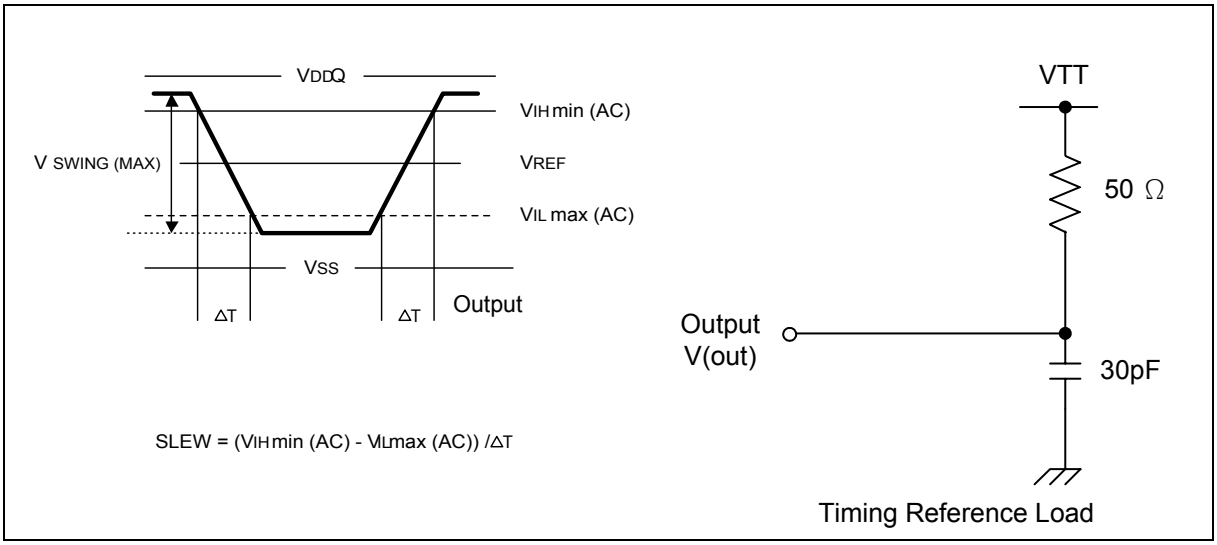
SYM.	PARAMETER		-4		-5/-5I		-6/-6I		UNIT	NOTES
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Active to Ref/Active Command Period		48		50		54		nS	
t_{RFC}	Ref to Ref/Active Command Period		60		70		70			
t_{RAS}	Active to Precharge Command Period		40	70000	40	100000	42	100000		
t_{RCDRD}	$\overline{RAS}$ to $\overline{CAS}$ delay for Read		5		4		3		t_{CK}	
t_{RCDWR}	$\overline{RAS}$ to $\overline{CAS}$ delay for Write		3		2		2			
t_{RAP}	Active to Read with Auto-precharge Enable		16		15		18		nS	
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1		1		1		t_{CK}	
t_{RP}	Precharge to Active Command Period		16		15		18		nS	
t_{RRD}	Active(a) to Active(b) Command Period		12		10		12			
t_{WR}	Write Recovery Time		3		3		2		t_{CK}	
t_{DAL}	Auto-precharge Write Recovery + Precharge Time		-		-		-			18
t_{CK}	CLK Cycle Time	CL = 2	-	-	7.5	12	7.5	12	nS	
		CL = 2.5	-	-	6	12	6	12		
		CL = 3	4	12	5	12	6	12		
		CL = 4	4	12	-	-	-	-		
t_{AC}	Data Access Time from CLK, $\overline{CLK}$		-0.6	0.6	-0.7	0.7	-0.7	0.7		16
t_{DQSCK}	DQS Output Access Time from CLK, $\overline{CLK}$		-0.6	0.6	-0.6	0.6	-0.6	0.6		
t_{DQSQ}	Data Strobe Edge to Output Data Edge Skew		-	0.4	-	0.4		0.4		
t_{CH}	CLk High Level Width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	11
t_{CL}	CLK Low Level Width		0.45	0.55	0.45	0.55	0.45	0.55		
t_{HP}	CLK Half Period (minimum of actual t_{CH}, t_{CL})		min (t_{CL},t_{CH})		min, (t_{CL},t_{CH})		min, (t_{CL},t_{CH})		nS	
t_{QH}	DQ Output Data Hold Time from DQS		t_{HP} -0.5		t_{HP} -0.5		t_{HP} -0.5			
t_{RPRE}	DQS Read Preamble Time		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	11
t_{RPST}	DQS Read Postamble Time		0.4	0.6	0.4	0.6	0.4	0.6		
t_{DS}	DQ and DM Setup Tim		0.4		0.4		0.4		nS	
t_{DH}	DQ and DM Hold Time		0.4		0.4		0.4			
t_{DIPW}	DQ and DM Input Pulse Width (for each input)		1.75		1.75		1.75			
t_{DQSH}	DQS Input High Pulse Width		0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	11
t_{DQSL}	DQS Input Low Pulse Width		0.4	0.6	0.4	0.6	0.4	0.6		
t_{DSS}	DQS Falling Edge to CLK Setup Time		0.2		0.2		0.2			
t_{DSH}	DQS Falling Edge Hold Time from CLK		0.2		0.2		0.2			
t_{WPRES}	Clock to DQS Write Preamble Set-up Time		0		0		0		nS	

AC Characteristics and Operating Condition, continued

SYM.	PARAMETER	-4		-5/-5I		-6/-6I		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WPREH}	Clock to DQS Write Preamble Hold Time	0.25		0.25		0.25		t_{CK}	11
t_{WPST}	DQS Write Postamble Time	0.4	0.6	0.4	0.6	0.4	0.6		
t_{DQSS}	Write Command to First DQS Latching Transition	0.72	1.25	0.72	1.25	0.75	1.25		
t_{IS}	Input Setup Time	0.75		0.75		0.8		nS	
t_{IH}	Input Hold Time	0.75		0.75		0.8			
t_{HZ}	Data-out High-impedance Time from CLK, $\overline{CLK}$		0.7		0.7		0.7		
t_{LZ}	Data-out Low-impedance Time from CLK, $\overline{CLK}$	-0.7	0.7	-0.7	0.7	-0.7	0.7		
$t_{T(SS)}$	SSTL Input Transition	0.5	1.5	0.5	1.5	0.5	1.5		
t_{WTR}	Internal Write to Read Command Delay	2		2		1		t_{CK}	
t_{XSNR}	Exit Self Refresh to non-Read Command	72		75		75		nS	
t_{XSRD}	Exit Self Refresh to Read Command	200		200		200		t_{CK}	
t_{REFi}	Refresh Interval Time (4K/64mS)		15.6		15.6		15.6	µS	17
t_{MRD}	Mode Register Set Cycle Time	8		10		12		nS	

9.7 AC Test Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Input High Voltage (AC)	V_{IH}	V_{REF} + 0.31	V
Input Low Voltage (AC)	V_{IL}	V_{REF} - 0.31	V
Input Reference Voltage	V_{REF}	0.5 x V_{DDQ}	V
Termination Voltage	V_{TT}	0.5 x V_{DDQ}	V
Input Signal Peak to Peak Swing	V_{SWING}	1.0	V
Differential Clock Input Reference Voltage	V_R	V_x (AC)	V
Input Difference Voltage. CLK and $\overline{CLK}$ Inputs (AC)	V_{ID} (AC)	1.5	V
Input Signal Minimum Slew Rate	SLEW	1.0	V/nS
Output Timing Measurement Reference Voltage	V_{OTR}	0.5 x V_{DDQ}	V



Notes:

(1) Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}, V_{SSQ}. (2.5V±0.1V for DDR500)

(3) Peak to peak AC noise on V_{REF} may not exceed ±2% $V_{REF(DC)}$.

(4) V_{OH} = 1.95V, V_{OL} = 0.35V

(5) V_{OH} = 1.9V, V_{OL} = 0.4V

(6) The values of $I_{OH(DC)}$ is based on V_{DDQ} = 2.3V and V_{TT} = 1.19V.
The values of $I_{OL(DC)}$ is based on V_{DDQ} = 2.3V and V_{TT} = 1.11V.

(7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

(8) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

(9) These parameters depend on the output loading. Specified values are obtained with the output open.

(10) Transition times are measured between $V_{IH\ min(AC)}$ and $V_{IL\ max(AC)}$.Transition (rise and fall) of input signals have a fixed slope.

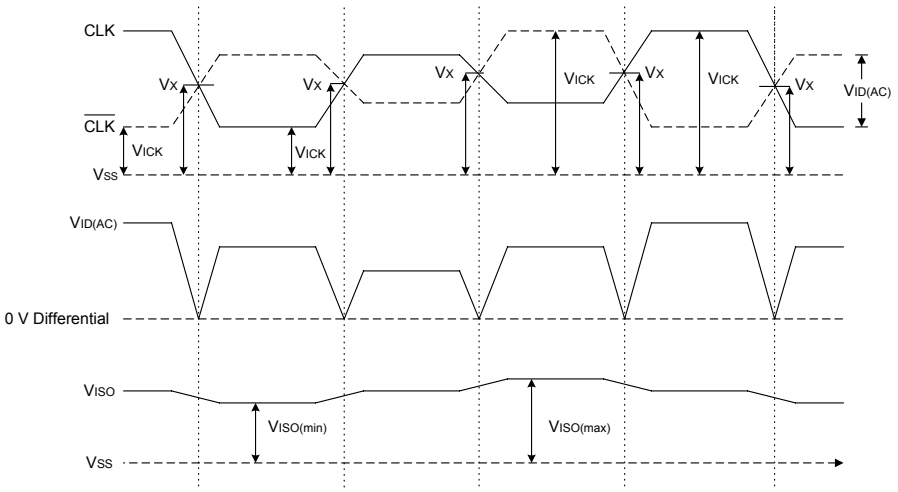
(11) IF the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., t_{DQSS} = 0.75 × t_{CK}, t_{CK} = 7.5 nS, 0.75 × 7.5 nS = 5.625 nS is rounded up to 5.6 nS.)

(12) V_X is the differential clock cross point voltage where input timing measurement is referenced.

(13) V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(14) V_{ISO} means {V_{ICK}(CLK)+V_{ICK}($\overline{CLK}$)}/2.

(15) Refer to the figure below.



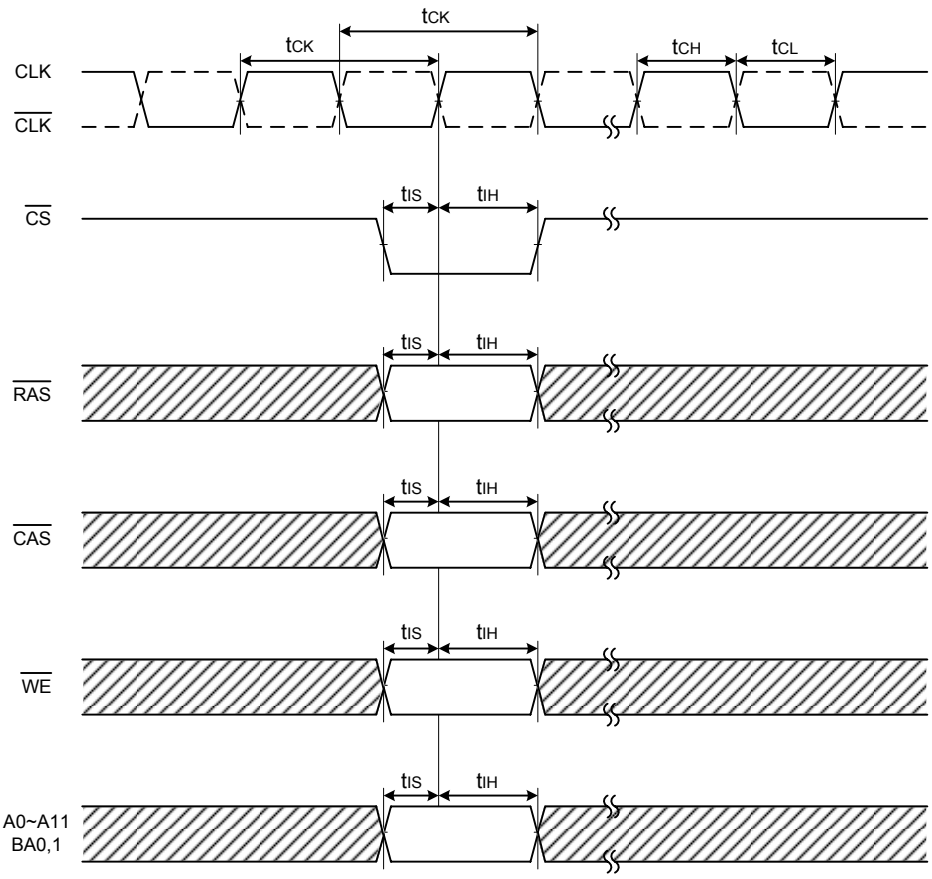
(16) t_{AC} and t_{DQSCK} depend on the clock jitter. These timing are measured at stable clock.

(17) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

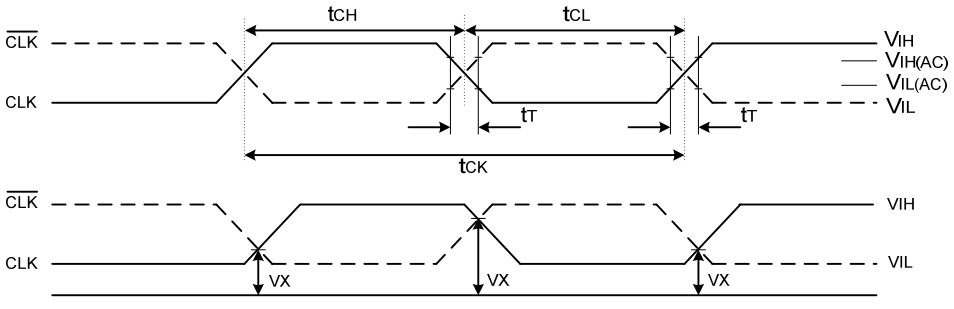
(18) $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$

10. TIMING WAVEFORMS

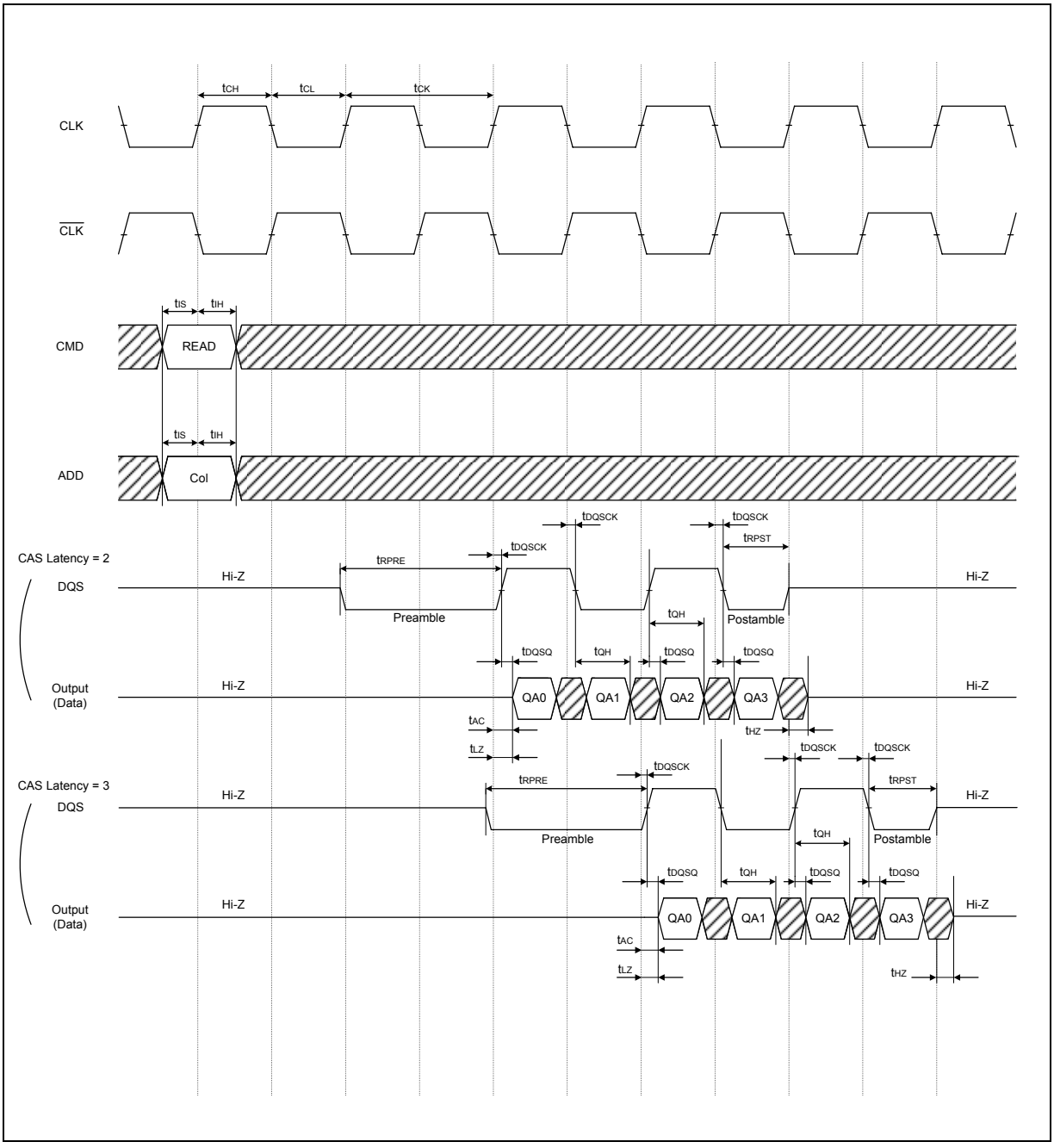
10.1 Command Input Timing



10.2 Timing of the CLK Signals



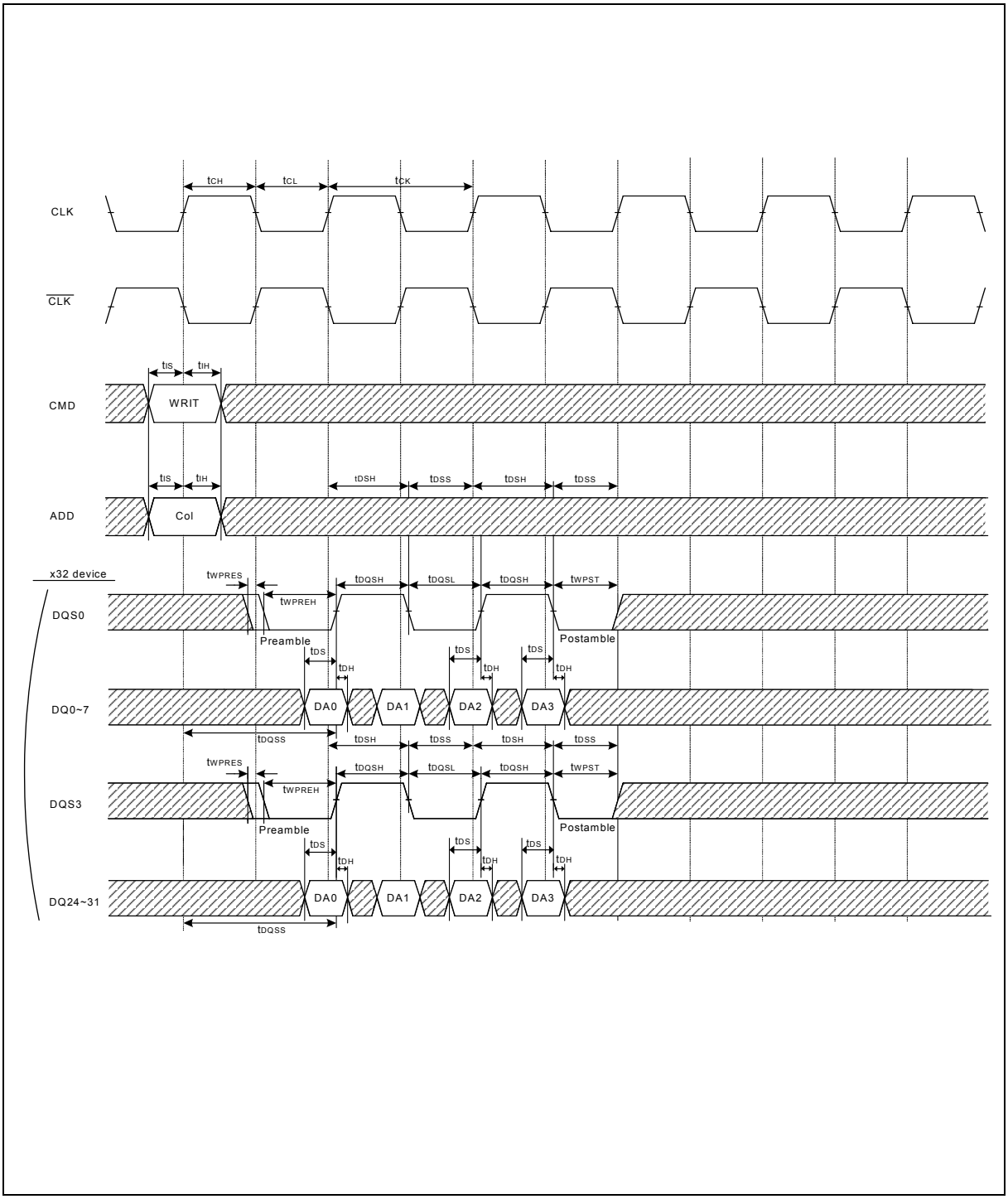
10.3 Read Timing (Burst Length = 4)



Notes: The correspondence of DQS0–DQS3 to DQ. (W9412G2IB)

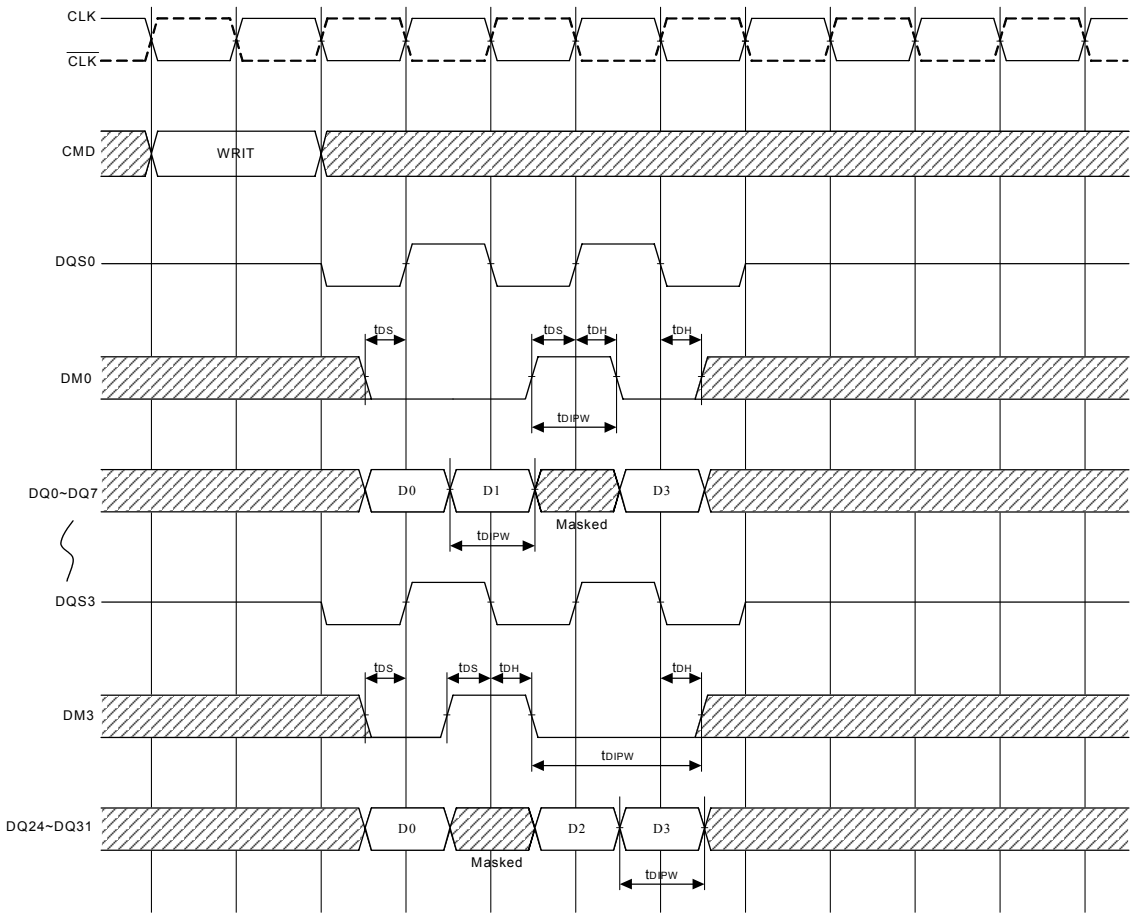
DQS0	DQ0–7
DQS1	DQ8–15
DQS2	DQ16–23
DQS3	DQ24–31

10.4 Write Timing (Burst Length = 4)

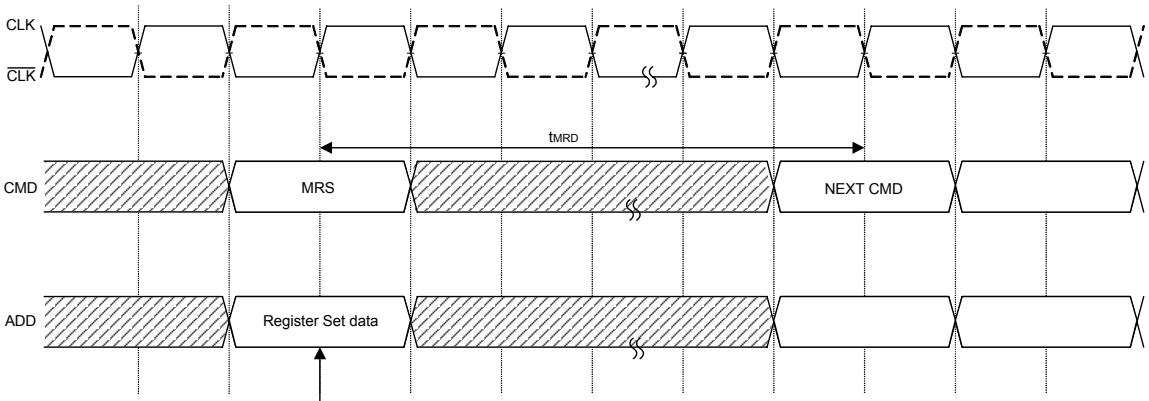


Note: x32 has four DQSs. (DQS0 for lower byte and DQS3 for upper byte)

10.5 DM, DATA MASK (W9412G2IB)



10.6 Mode Register Set (MRS) Timing



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	Reserved
A8	DLL Reset	
A9	"0"	Reserved
A10	"0"	
A11	"0"	
BA0	"0"	Mode Register Set or Extended Mode Register Set
BA1	"0"	

* "Reserved" should stay "0" during MRS cycle.

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1		

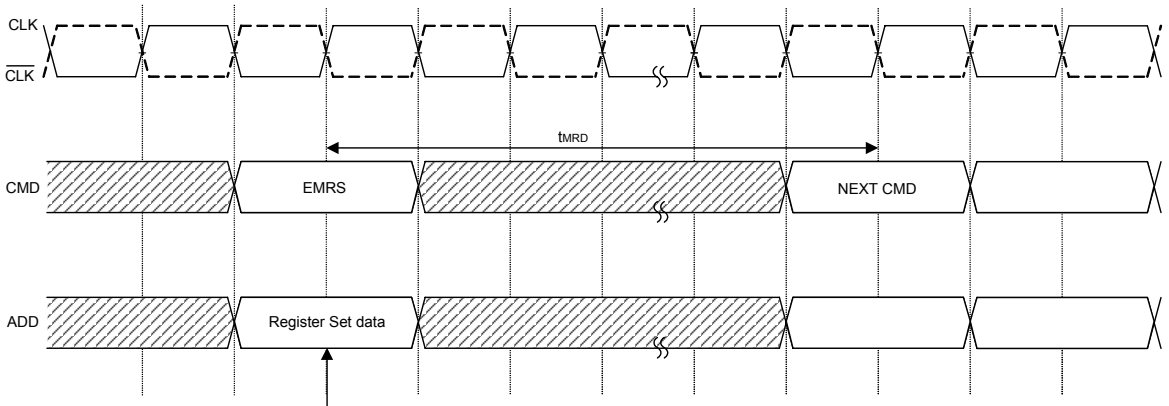
A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A8	DLL Reset
0	No
1	Yes

BA1	BA0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

10.7 Extend Mode Register Set (EMRS) Timing



A0	DLL Switch	
A1	Buffer Strength	
A2	"0"	Reserved
A3	"0"	
A4	"0"	
A5	"0"	
A6	"0"	Buffer Strength
A7	"0"	Reserved
A8	"0"	
A9	"0"	
A10	"0"	
A11	"0"	
BA0	"0"	Mode Register Set or Extended Mode Register Set
BA1	"0"	

A0	DLL Switch
0	Enable
1	Disable

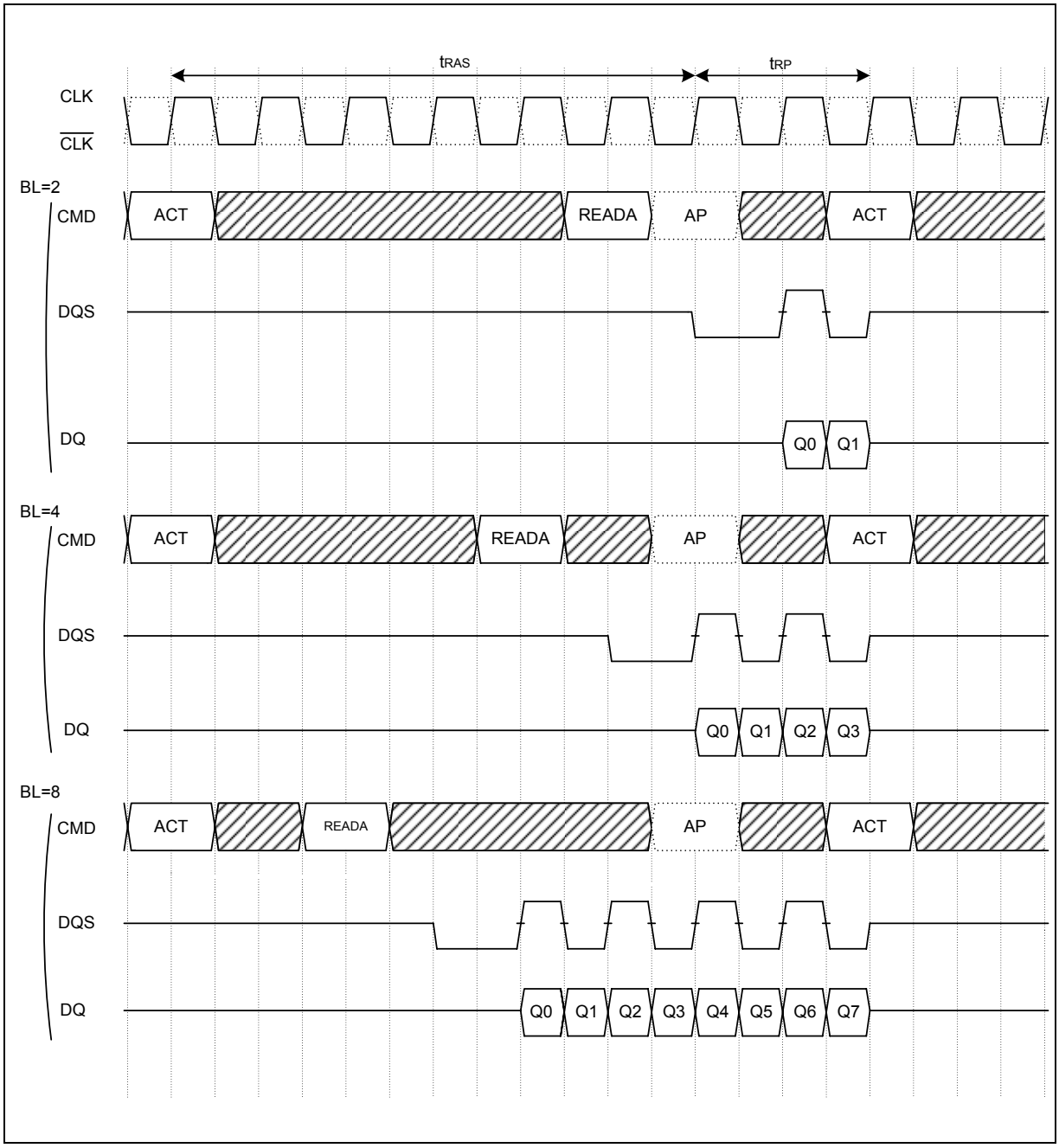
A6	A1	Buffer Strength
0	0	100% Strength
0	1	60% Strength
1	0	Reserved
1	1	30% Strength

BA1	BA0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	
1	1	

* "Reserved" should stay "0" during EMRS cycle.

10.8 Auto-precharge Timing (Read Cycle, CL = 2)

1) tRCD (READA) ≥ tRAS (min) – (BL/2) × tCK



Notes: CL=2 shown; same command operation timing with CL=2.5 and CL=3

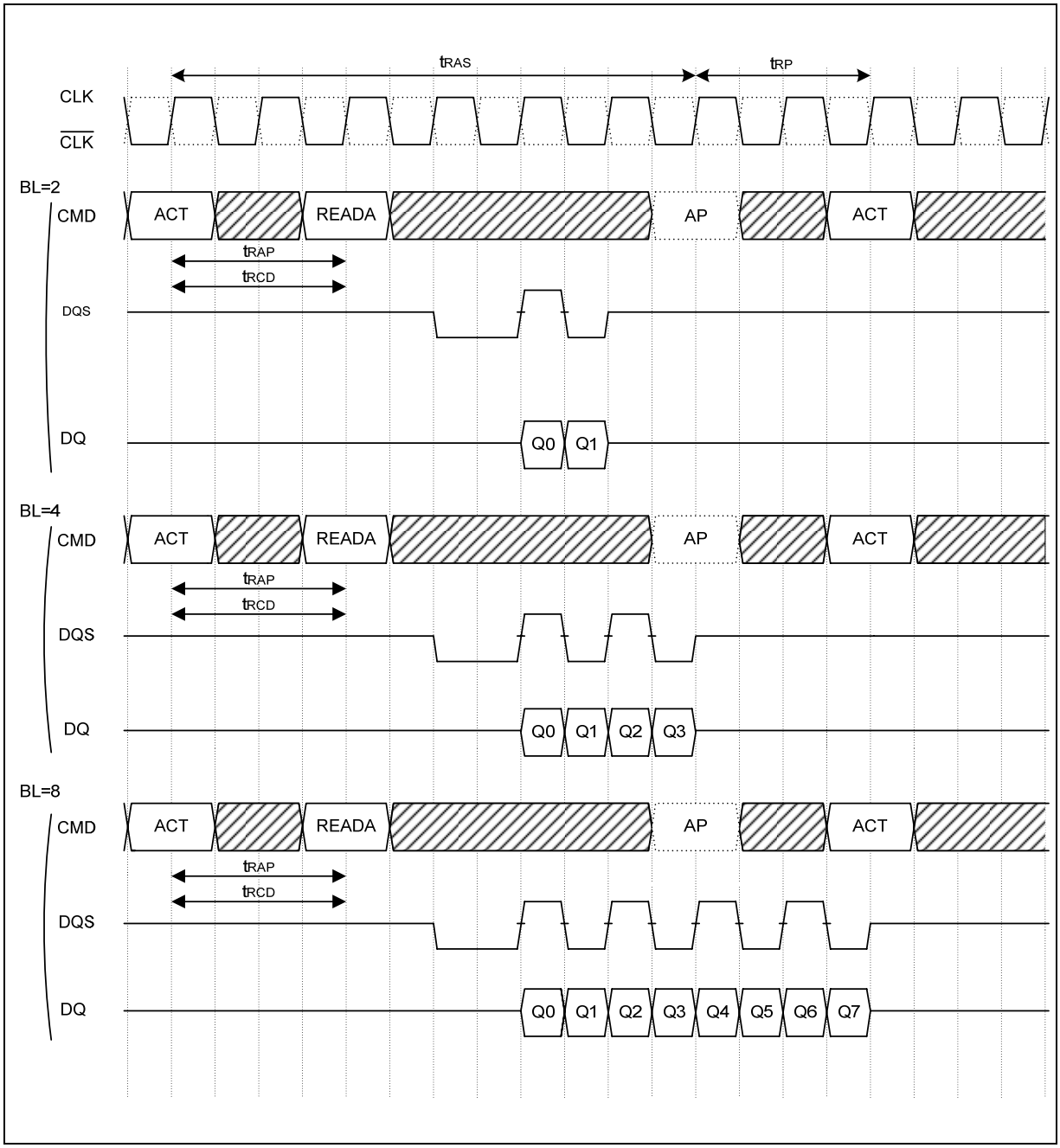
In this case, the internal precharge operation begin after BL/2 cycle from READA command.

AP Represents the start of internal precharging.

The Read with Auto-precharge command cannot be interrupted by any other command.

10.9 Auto-precharge Timing (Read cycle, CL = 2), continued

2) tRCD/RAP(min) ≤ tRCD (READA) < tRAS (min) – (BL/2) × tCK



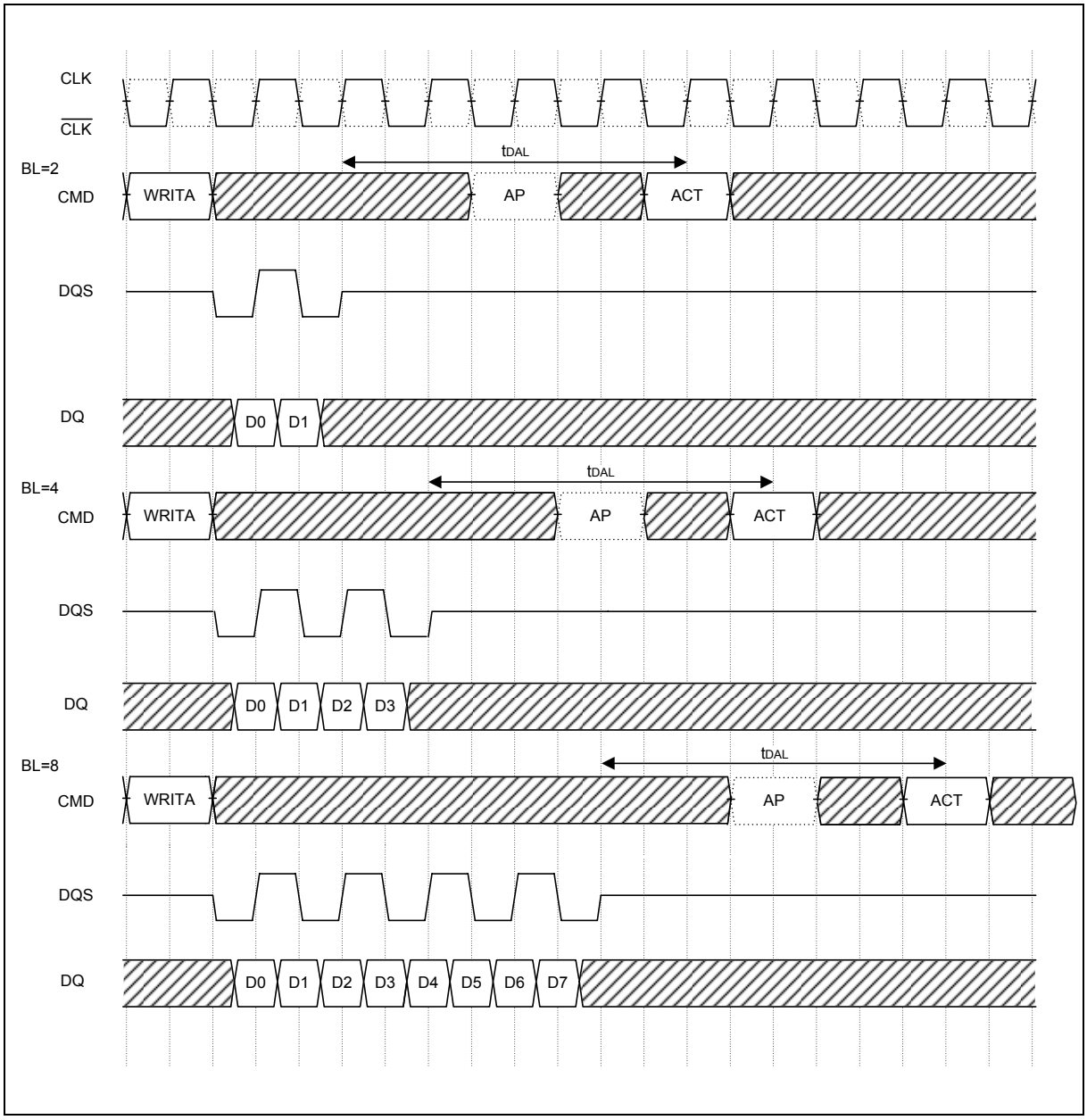
Notes: CL2 shown; same command operation timing with CL = 2.5, CL=3.

In this case, the internal precharge operation does not begin until after tRAS (min) has command.

AP Represents the start of internal precharging.

The Read with Auto-precharge command cannot be interrupted by any other command.

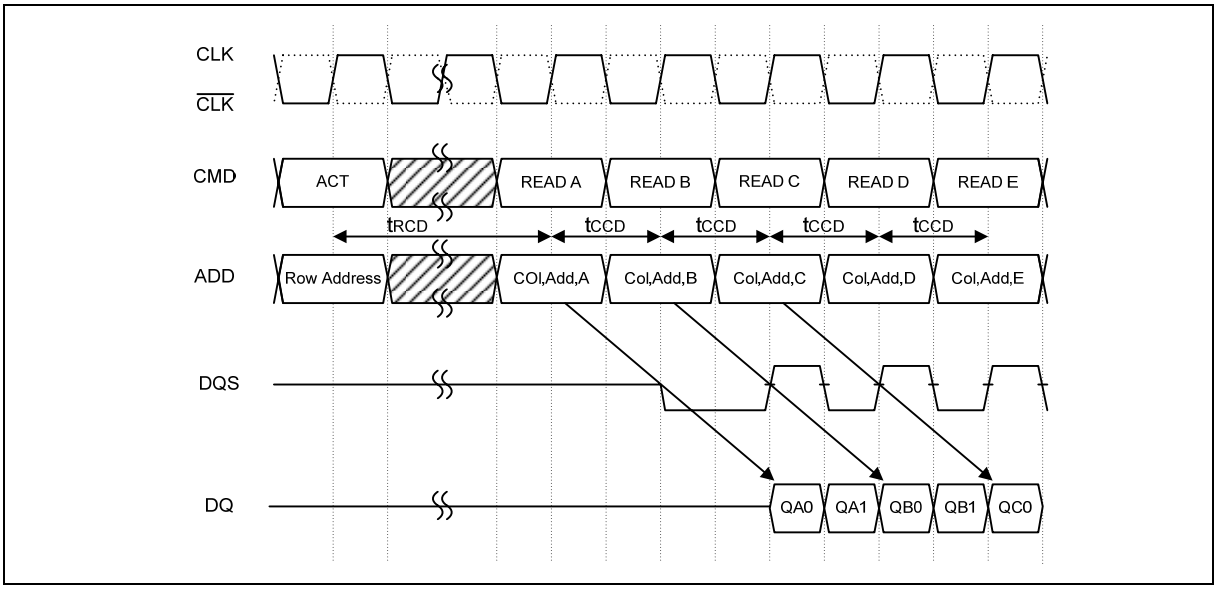
10.10 Auto-precharge Timing (Write Cycle)



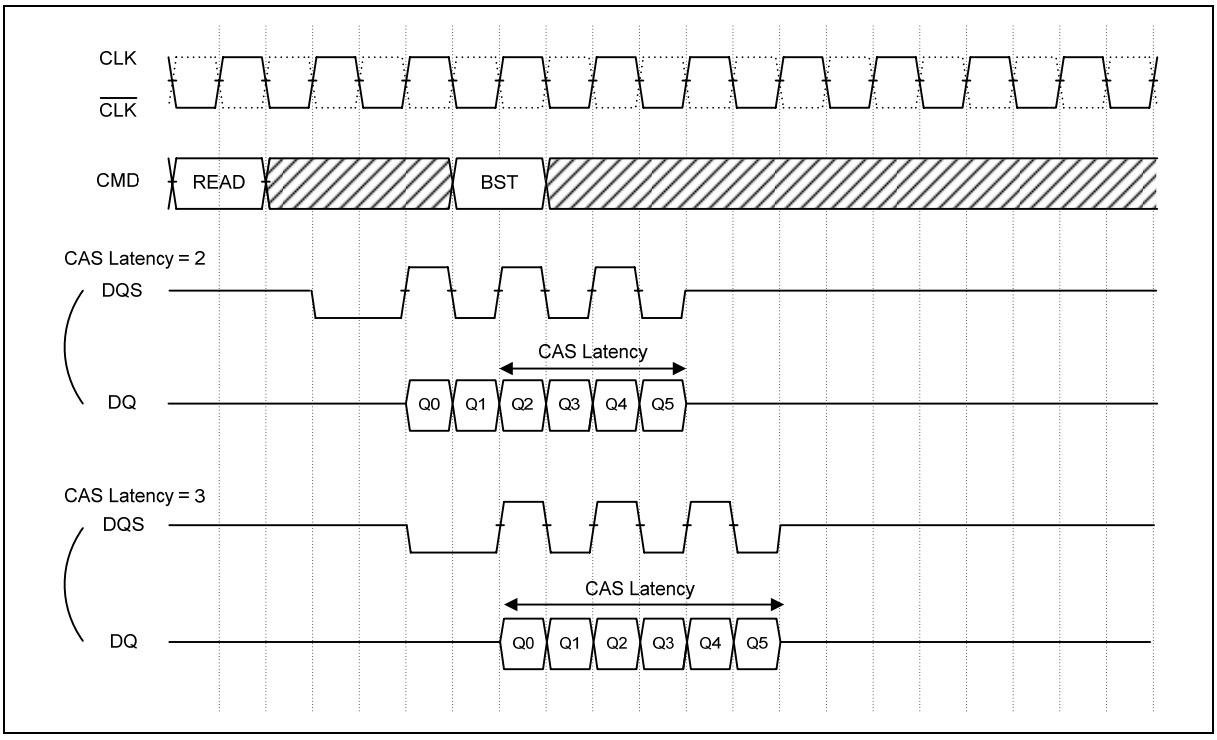
The Write with Auto-precharge command cannot be interrupted by any other command.

AP Represents the start of internal precharging.

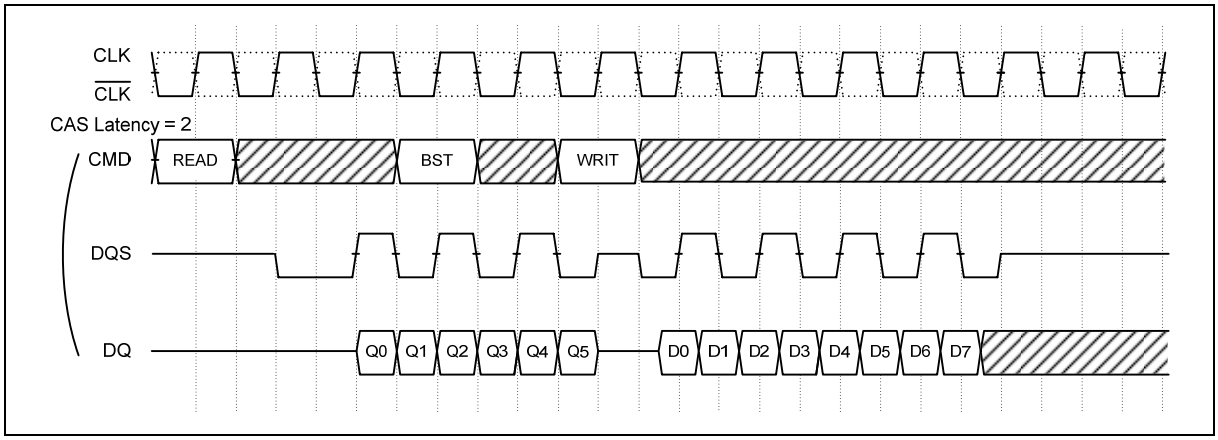
10.11 Read Interrupted by Read (CL = 2, BL = 2, 4, 8)



10.12 Burst Read Stop (BL = 8)

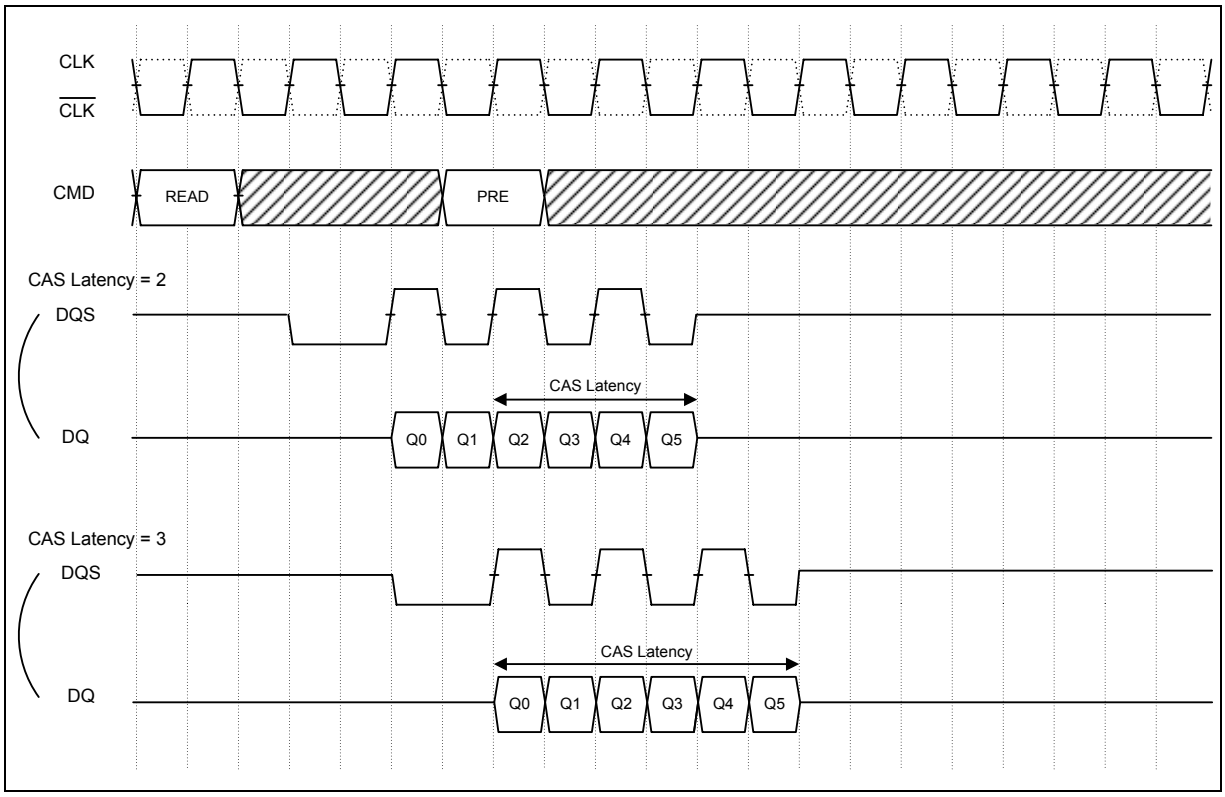


10.13 Read Interrupted by Write & BST (BL = 8)

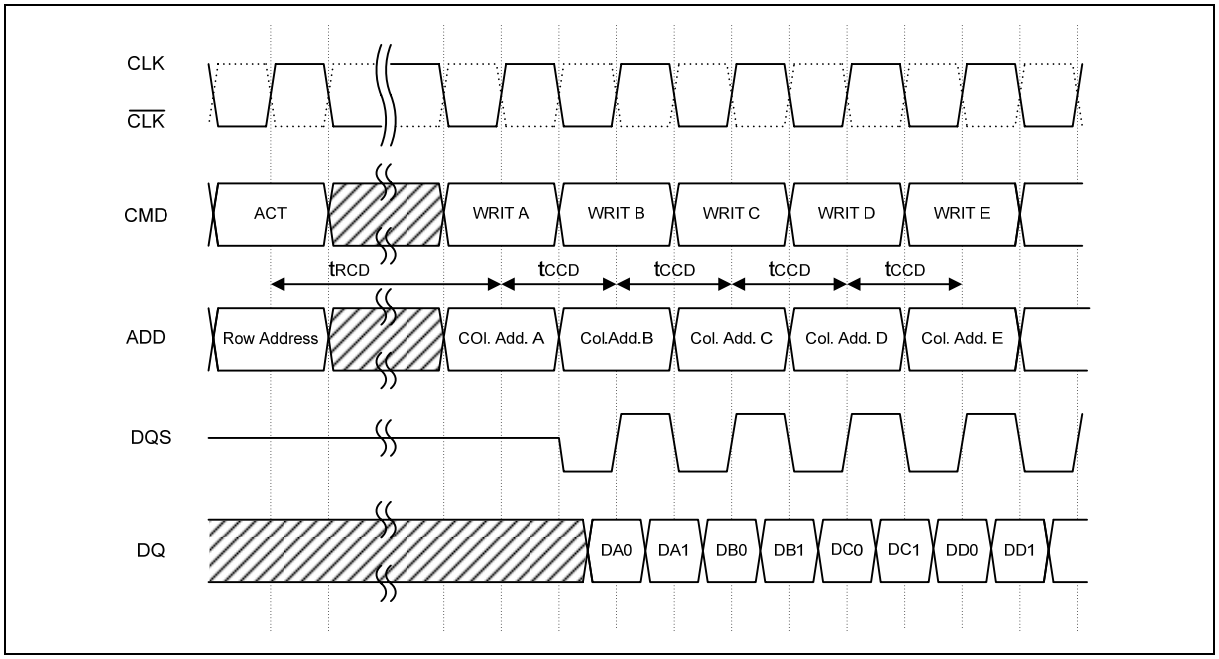


Burst Read cycle must be terminated by BST Command to avoid I/O conflict.

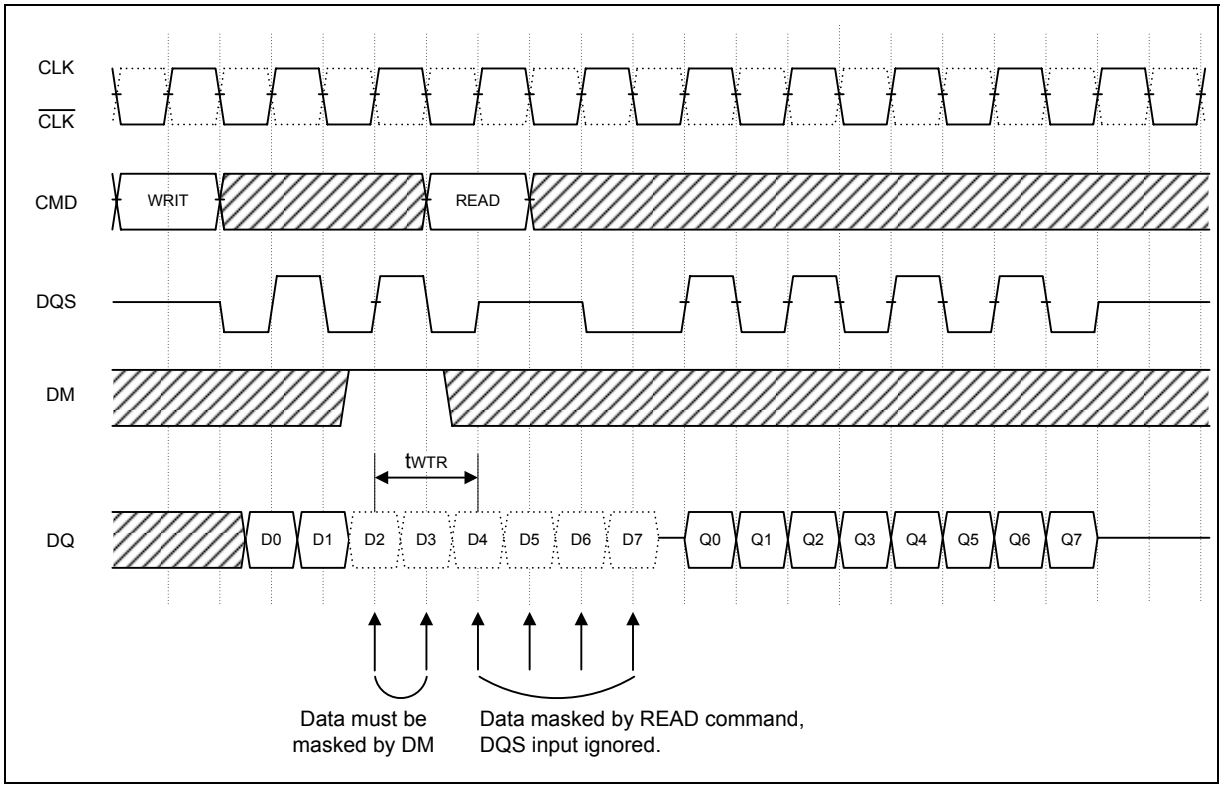
10.14 Read Interrupted by Precharge (BL = 8)



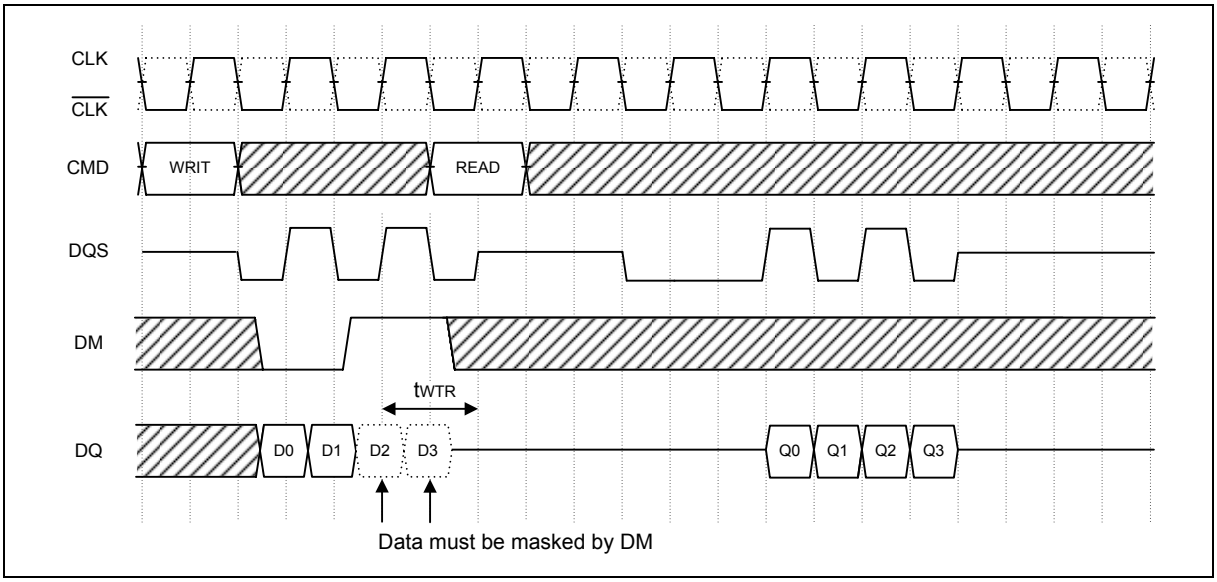
10.15 Write Interrupted by Write (BL = 2, 4, 8)



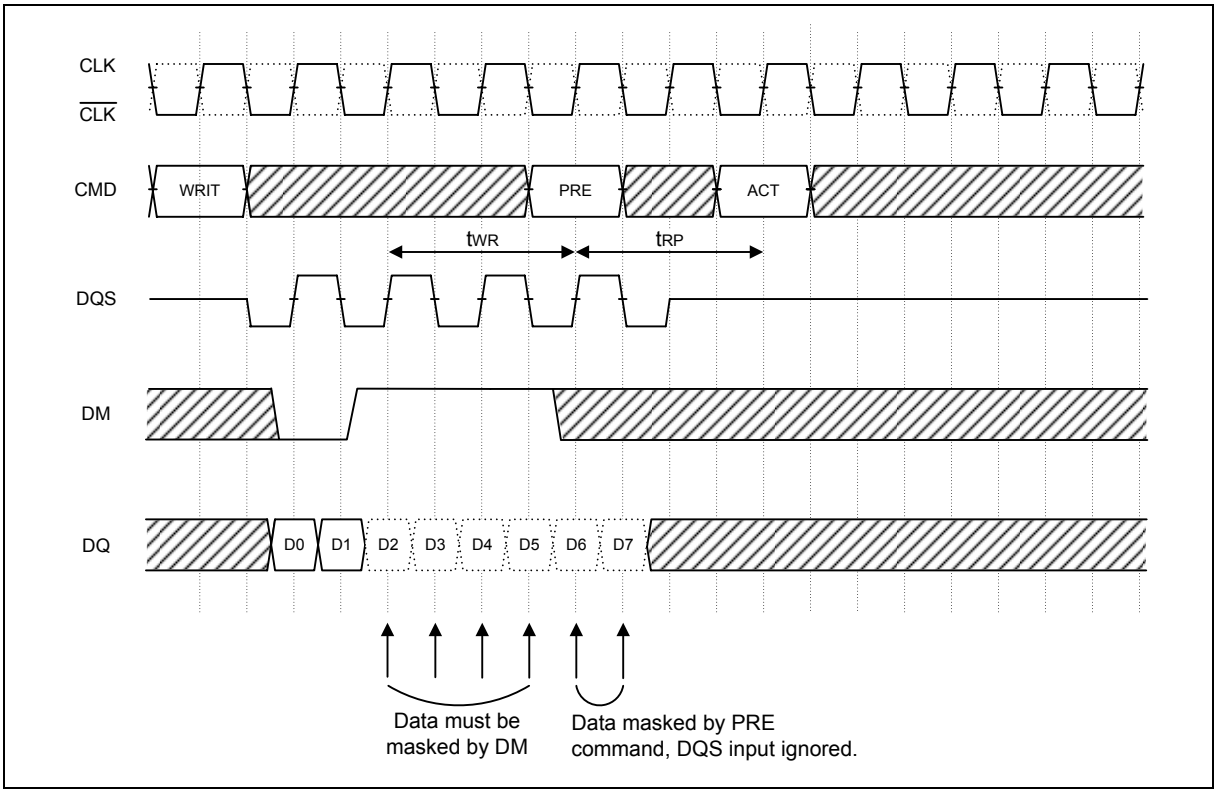
10.16 Write Interrupted by Read (CL = 2, BL = 8)



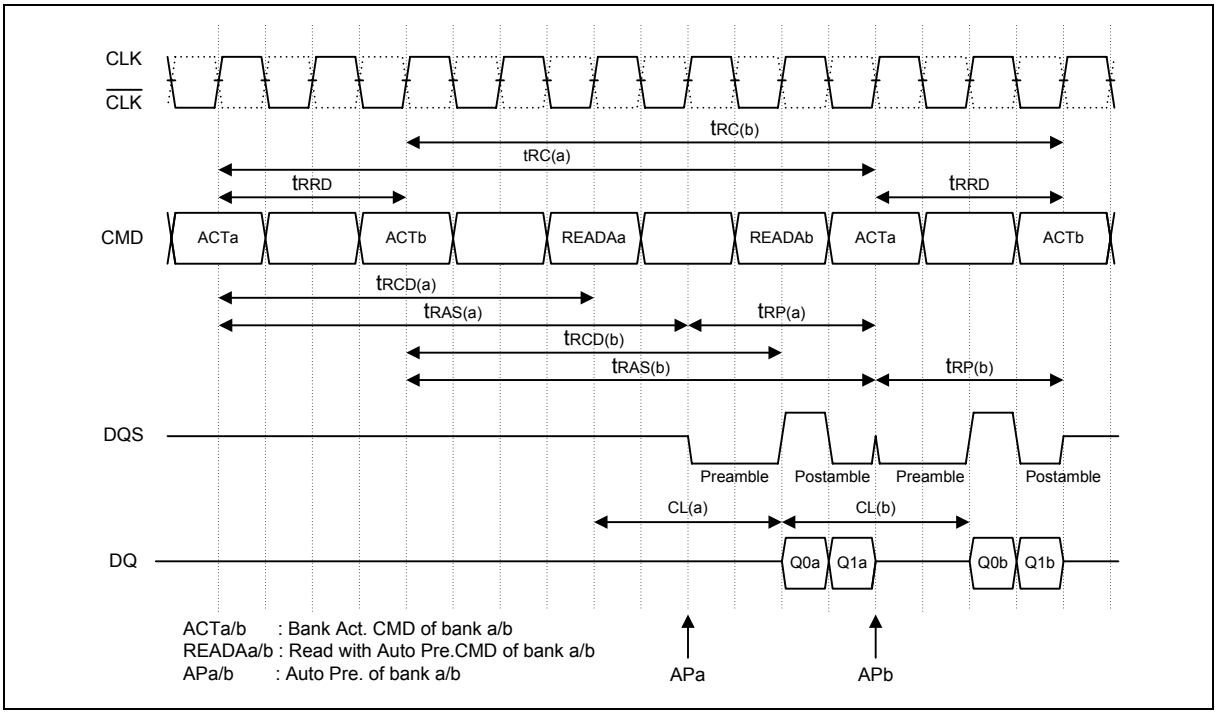
10.17 Write Interrupted by Read (CL = 3, BL = 4)



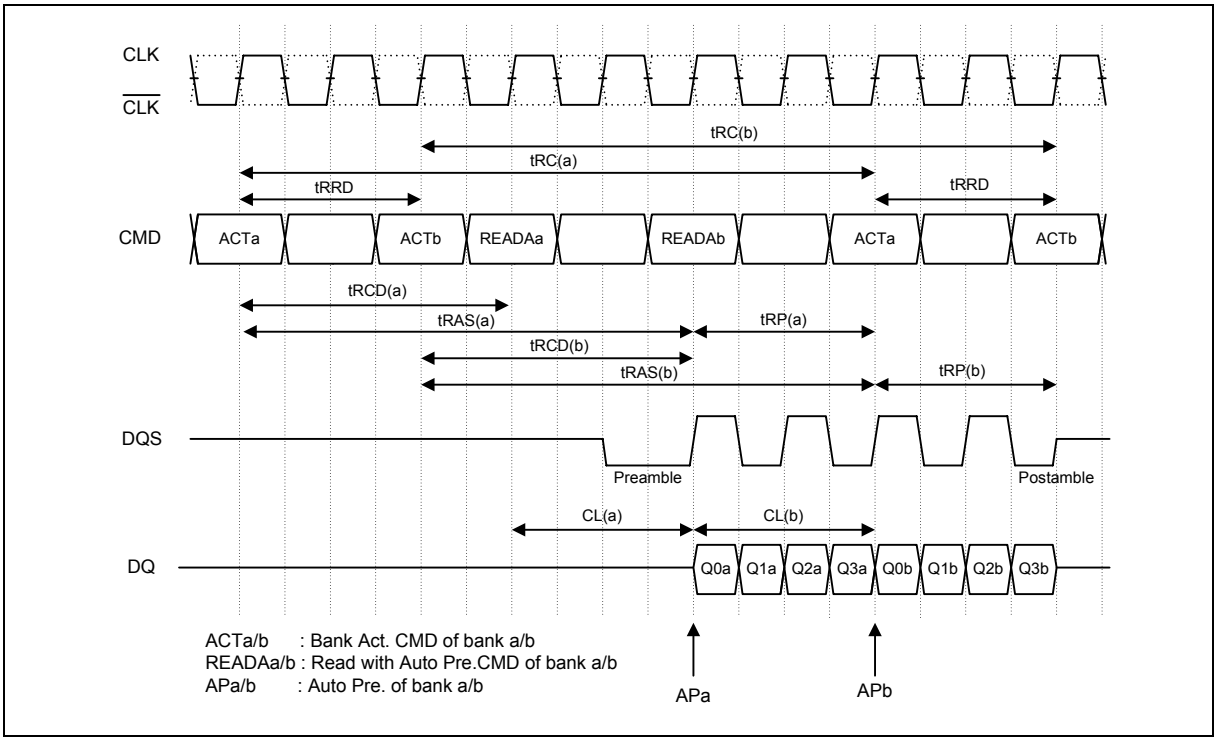
10.18 Write Interrupted by Precharge (BL = 8)



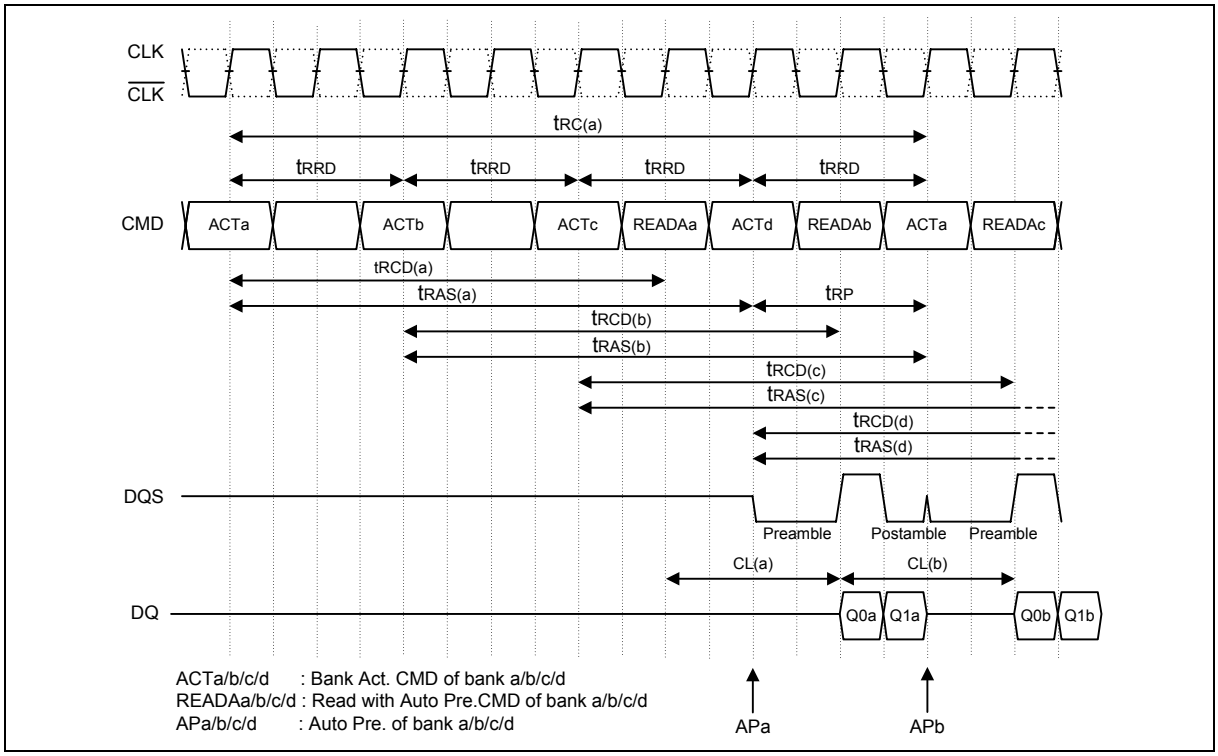
10.19 2 Bank Interleave Read Operation (CL = 2, BL = 2)



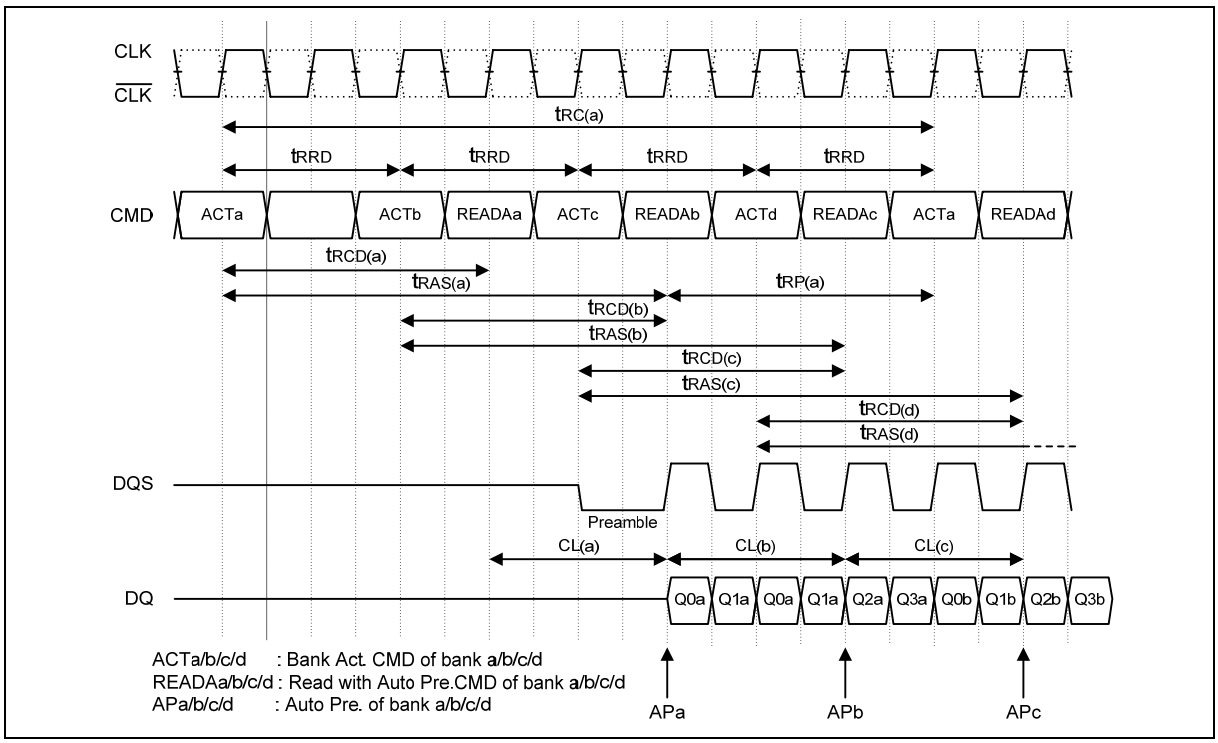
10.20 2 Bank Interleave Read Operation (CL = 2, BL = 4)



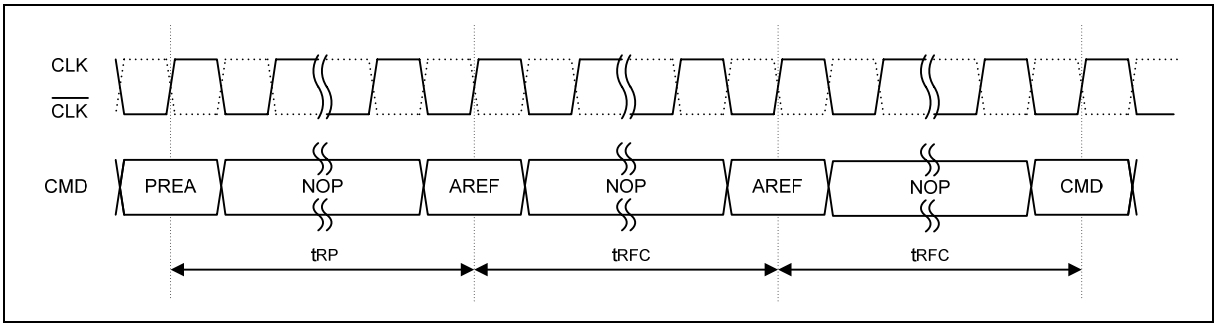
10.21 4 Bank Interleave Read Operation (CL = 2, BL = 2)



10.22 4 Bank Interleave Read Operation (CL = 2, BL = 4)

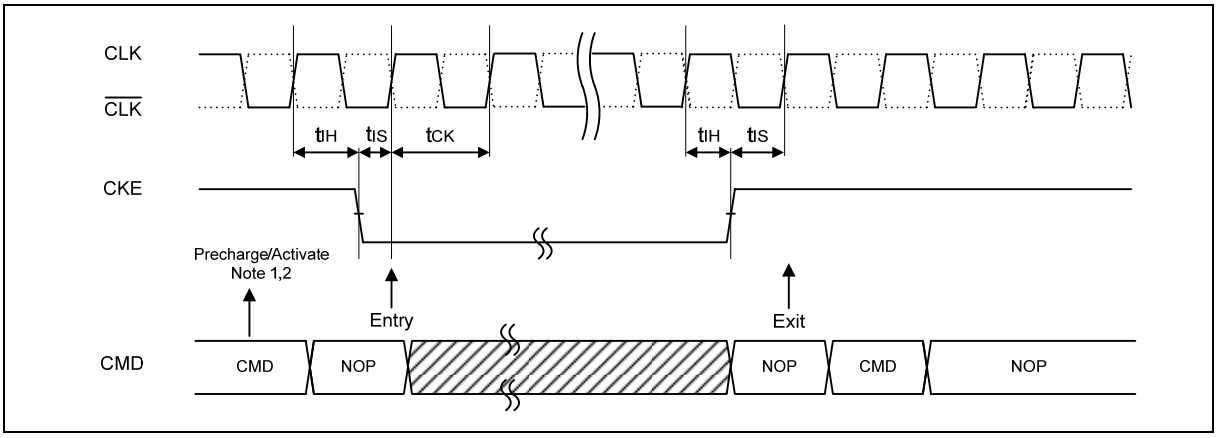


10.23 Auto Refresh Cycle



Note: CKE has to be kept "High" level for Auto-Refresh cycle.

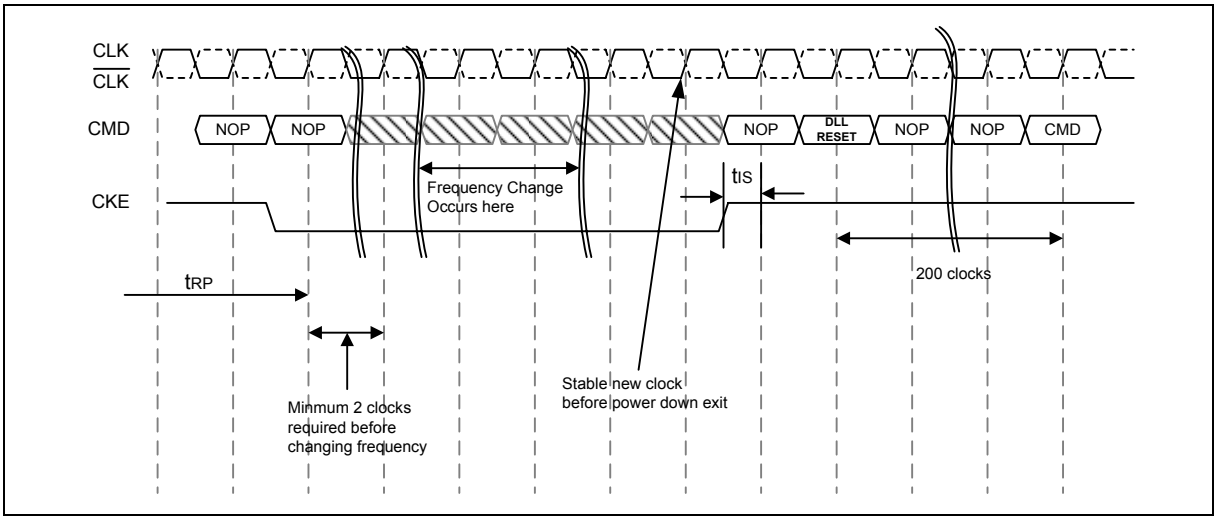
10.24 Precharge/Activate Power Down Mode Entry and Exit Timing



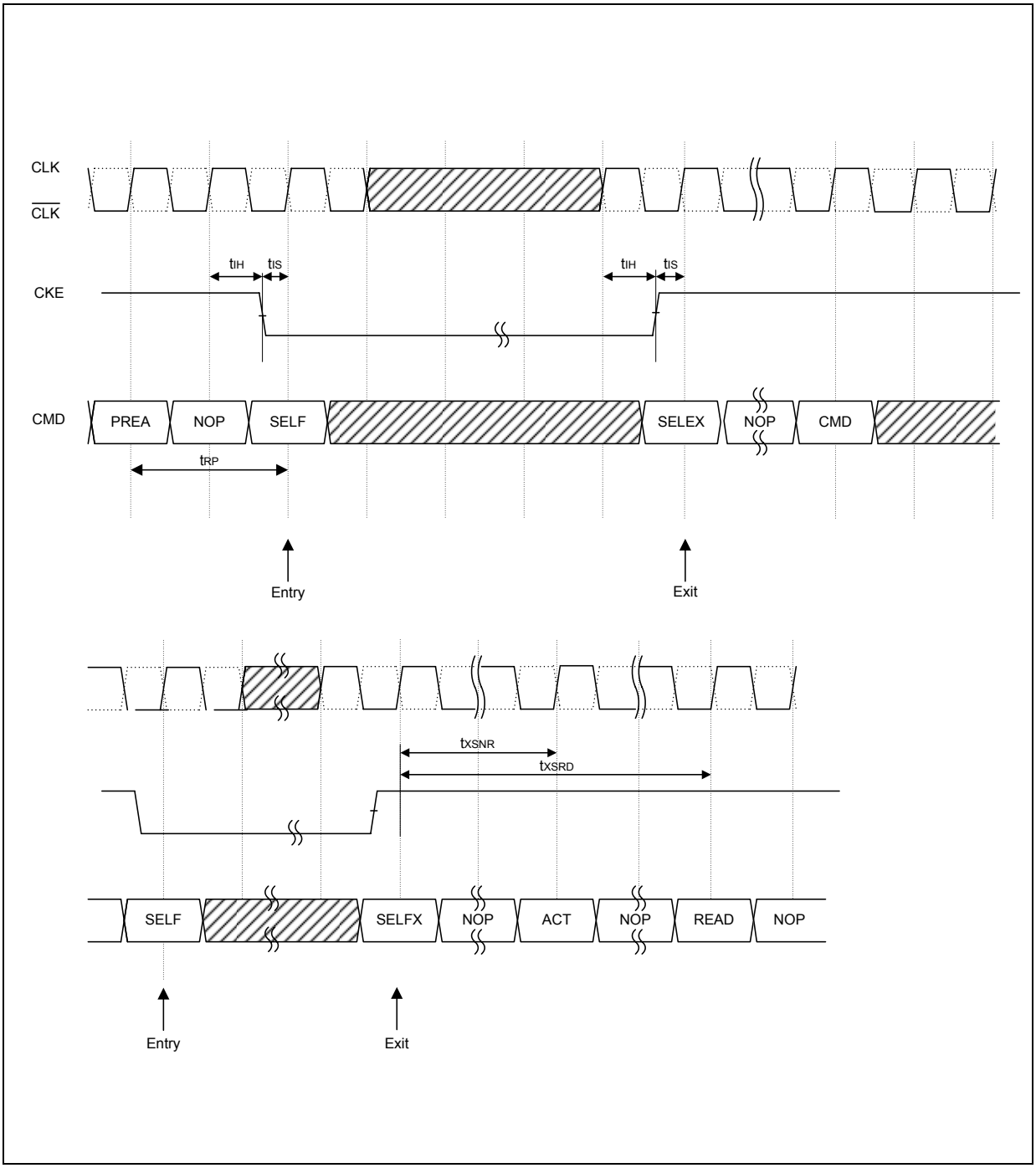
Note:

1. If power down occurs when all banks are idle, this mode is referred to as precharge power down.
2. If power down occurs when there is a row active in any bank, this mode is referred to as active power down.

10.25 Input Clock Frequency Change during Precharge Power Down Mode Timing



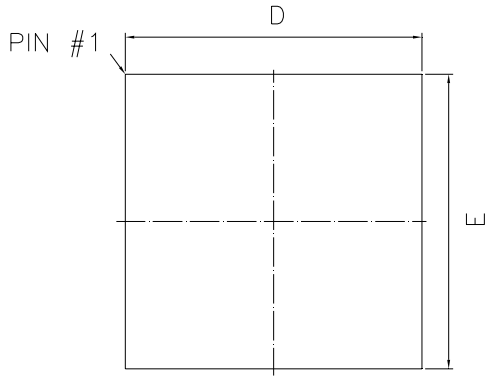
10.26 Self Refresh Entry and Exit Timing

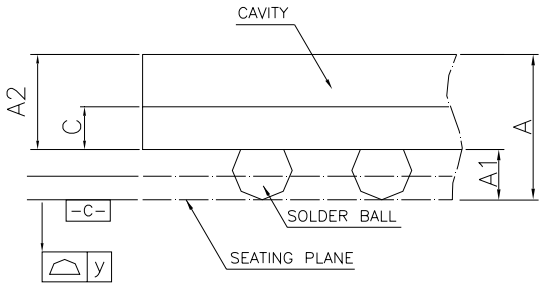


Note: If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.

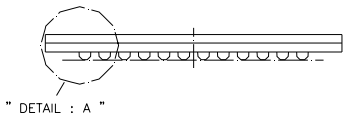
11. PACKAGE SPECIFICATION

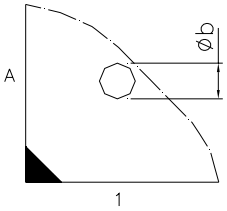
11.1 144L LFBGA (12X12X1.40 mm^3, Ø=0.5mm)



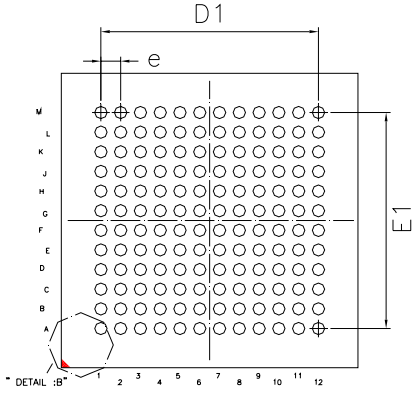


DETAIL : A



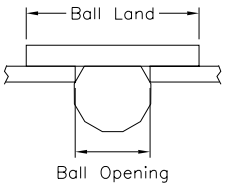


DETAIL : B



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.45	0.50	0.55	0.018	0.020	0.022
y	0.12			0.005		

Note: Ball Land: 0.55mm / Ball opening: 0.45m



12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Aug. 19, 2008	All	Initial formally data sheet
A02	Sep. 18, 2008	28	Revise typo error of t_{RCDRD}/t_{RCDWR} AC parameters unit change the unit from nS to t_{CK}
A03	Nov. 20, 2008	5, 27	Revise all speed grade DC parameter, I_{DDx} values
A04	Apr. 20, 2009	4, 25, 30	Revise -4 speed grade power supply voltage range from 2.6V ±0.1V to 2.5V ±0.1V
A05	May 27, 2009	4, 5, 25, 27~29	Add -6I industrial grade parts
A06	Aug. 30, 2010	4, 5, 25, 27~29	Add -5I industrial grade parts